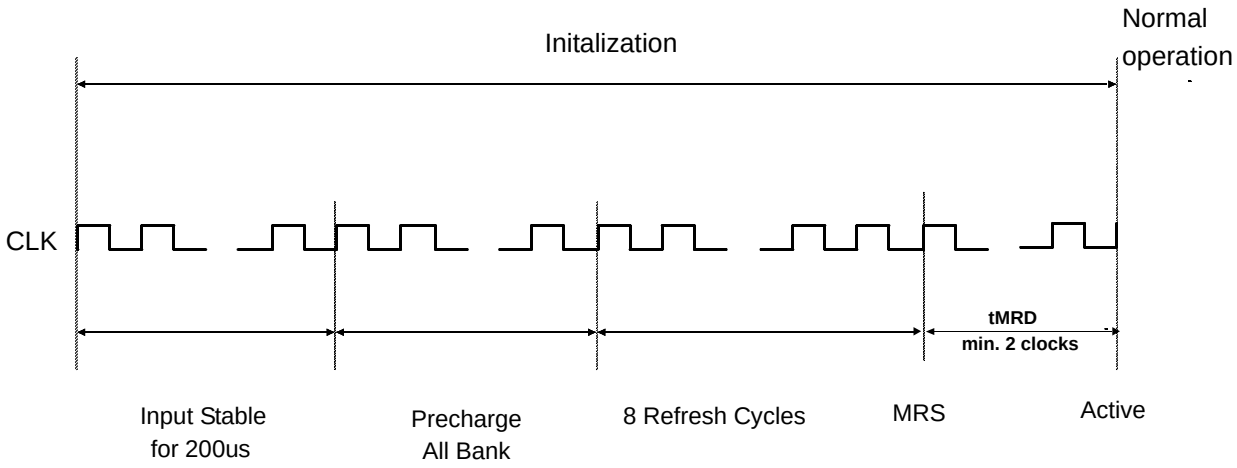
POWER UP SEQUENCE

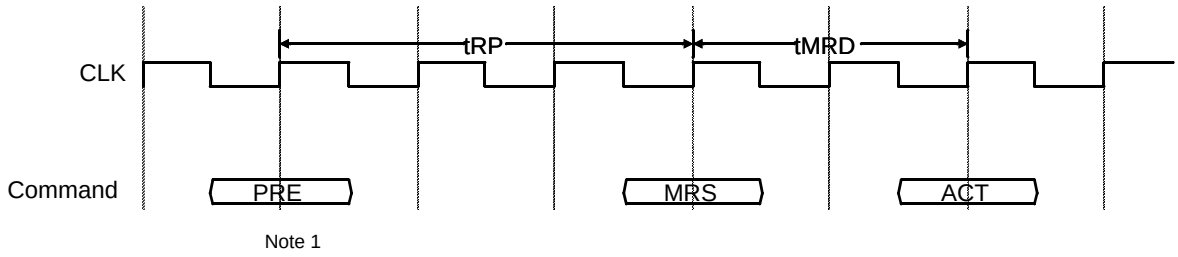
SDRAM must be initialized with the proper power-up sequence to the following (JEDEC Standard 21C 3.11.5.4):

1. Apply power and start clock. Attempt to maintain a NOP condition at the inputs
2. Maintain stable power, stable clock, and a NOP condition for a minimum of 200us
3. Issue precharge commands for all banks of the device
4. Issue 8 or more auto-refresh commands
5. Issue a mode register set command to initialize the mode register



MODE REGISTER SET

The SDRAM has an on-chip mode register which is programmed by the user to select the read latency, burst length, and burst type to be used during read/write operations to the DRAM. After power-up sequence, the MRS command must be issued to initialize the device. This command can be issued only when all banks are in idle state and CKE must be high at least one cycle before the Mode Register Set Command can be issued. This command is issued by the low signals of $\overline{RAS}$, $\overline{CAS}$, $\overline{CS}$ and $\overline{WE}$ at the positive edge of the clock and address pins are used to data input. Refer the MRS table for details. Two cycles are required to write the data in mode register. During the the MRS cycle, any command cannot be issued. If vendor want to modify functionality of device, it could be altered by re-programming through the MRS command.



Note : 1. All banks should be precharge state to excute MRS command

ROW ACTIVE

A random row in the idle bank of SDRAM can be activated using a bank active command. The bank active command is initiated by activating $\overline{CS}$, $\overline{RAS}$ and deactivating $\overline{CAS}$, $\overline{WE}$ with row and bank address at the same clock rising edge. Once a row active command has been issued to the bank selected by the bank address, the selected bank leaves its idle state and goes into its row activating state. Accordingly, the row address is latched and the appropriate row in the bank selected. Data from that row of memory is sensed and latched by the bank`s sense amplifiers, to be used for later read or write operations. Burst read or write command can be issued on the this activated row after the minimum tRCD time delay. A bank can be activated even when the opposite bank is active. Minimun tRRD time delay is required to active anonther bank. A row active command cannot be given to a bank if that bank is already active. Also, a row active command cannot be given to either bank if the SDRAM is currently in the power down, self refresh, auto refresh (for the period specified by tRC), or clock suspend states.

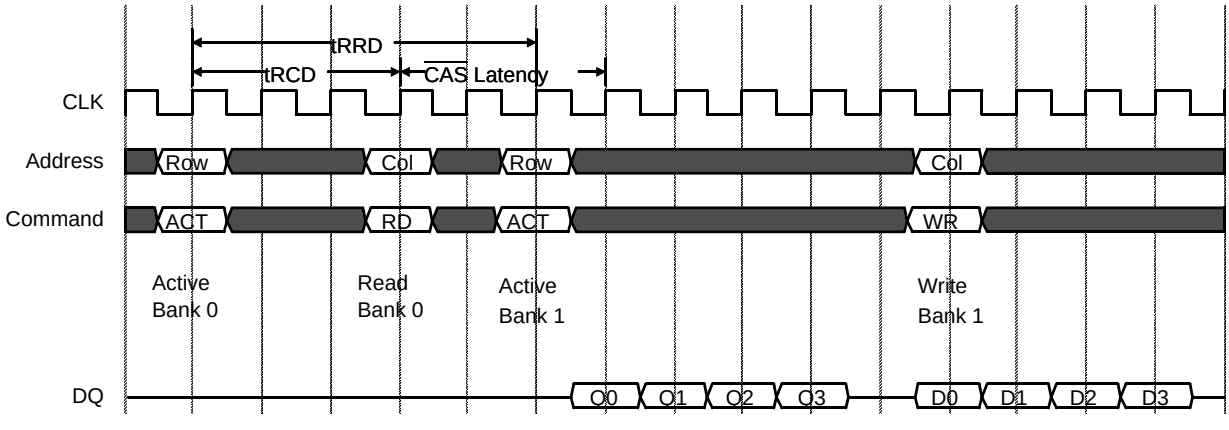
READ BANK

This command is used to access burst read of data in actived row. The read command is initiated by activating $\overline{CS}$, $\overline{CAS}$ and asserting high on $\overline{WE}$ with column address at the same clock rising edge. The first data is available after $\overline{CAS}$ latency number of clock cycles. The length of the burst and the $\overline{CAS}$ latency will be determined by mode register set values. The burst read can be terminated by another commands - burst stop, burst read or burst write command to the same bank or the other active bank or a precharge command to the same bank. At the end of burst length, the data outputs will go to Hi-Z and the bank will re-enter the row active state.

WRITE BANK

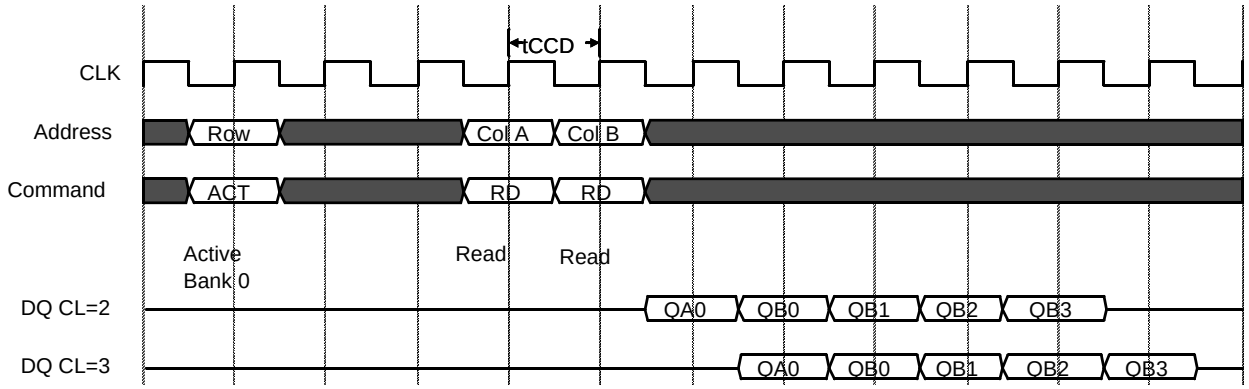
This command is used to write data into SDRAM. The write command is initiated by activating $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ with column address at the same clock rising edge. The first data can be input with write command and column address in same clock cycle regardless of what value of $\overline{CAS}$ latency is programmed into the mode register. The length of the burst will be determined by the values programmed during the MRS command.

ROW ACTIVE, READ AND WRITE



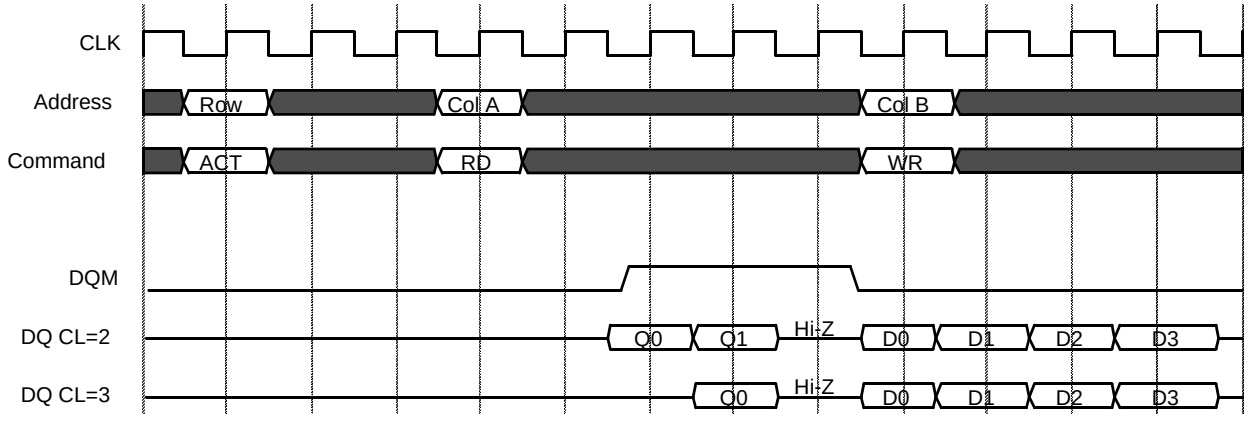
BL=4, CL=3 and tRCD=3

READ TERMINATED BY READ



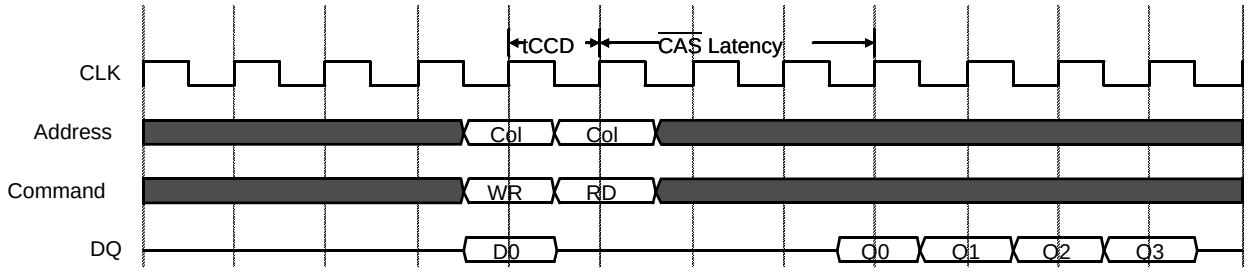
BL=4, CL=2

READ TERMINATED BY WRITE AND DQM



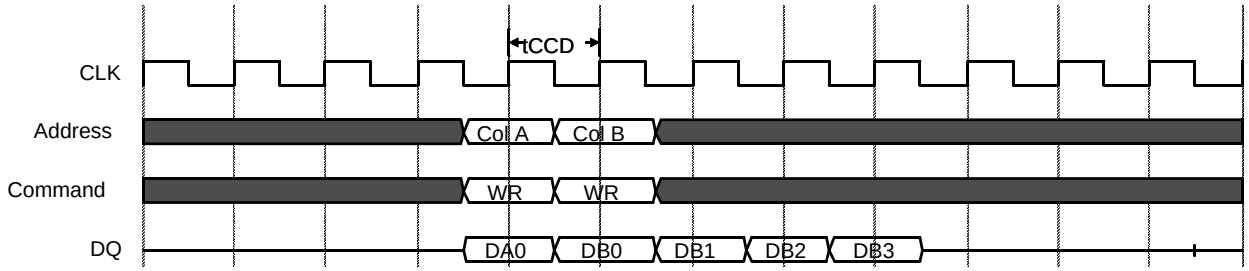
BL=4

WRITE TERMINATED BY READ



BL=4, CL=3

WRITE TERMINATED BY WRITE

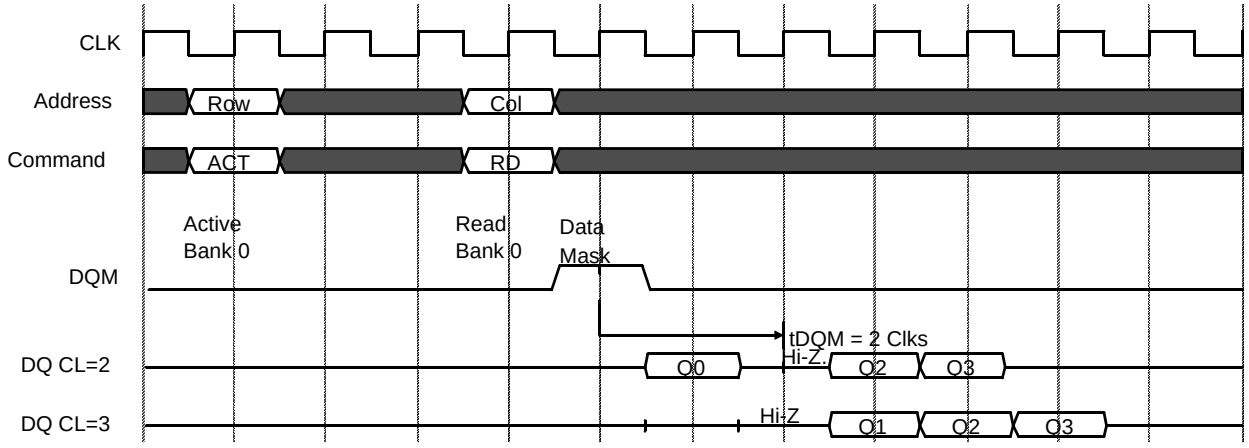


BL=4

DQM FUNCTION

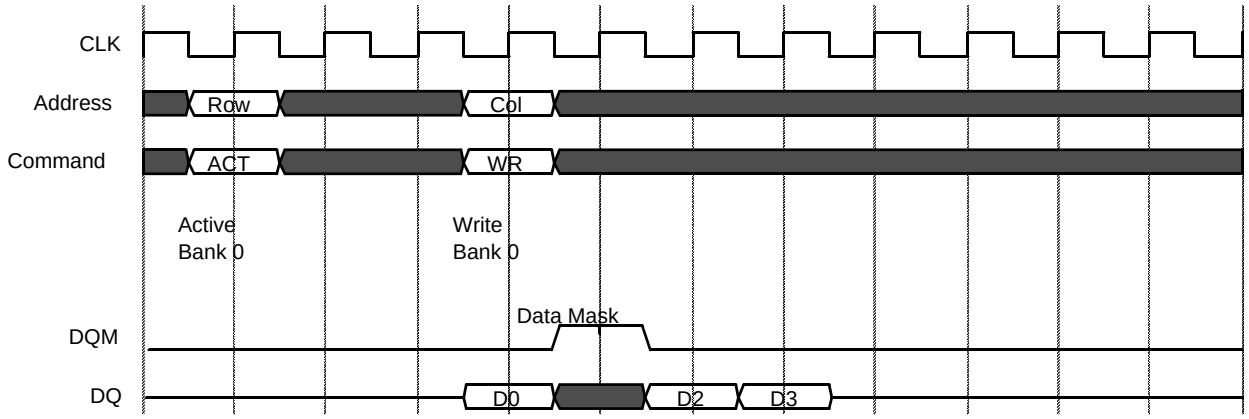
This command is used to mask data input during the write cycle and control output buffer during the read cycle. If data mask is initated by asserting low on DQM during the read cycle, the data outputs are masked (disabled) and become Hi-Z state after 2 cycle later. During the write cycle, DQM mask data input with zero latency.

READ DATA MASK



BL=4, CL=2 & 3

WRITE DATA MASK

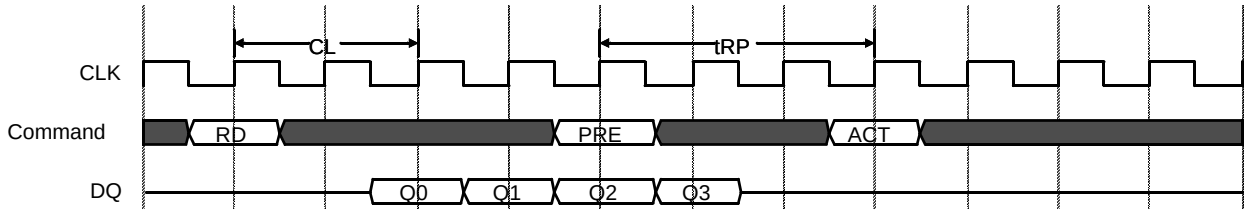


BL=4

PRECHARGE

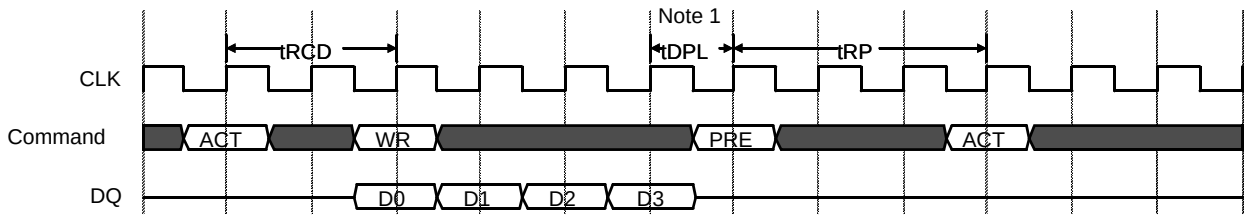
This command is used to precharge bank selected by bank addresses. The precharge command is initiated by activating $\overline{CS}$, $\overline{RAS}$, $\overline{WE}$ and AP with bank address. When AP is high, all banks are precharged by precharge command. When AP is low, only the bank which selected by bank address is precharged. After precharged command is issued, minimun tRP time delay must be required to active bank. After tRP timing delay, bank will be idle state.

PRECHARGE AFTER BURST READ



BL=4

PRECHARGE AFTER BURST WRITE



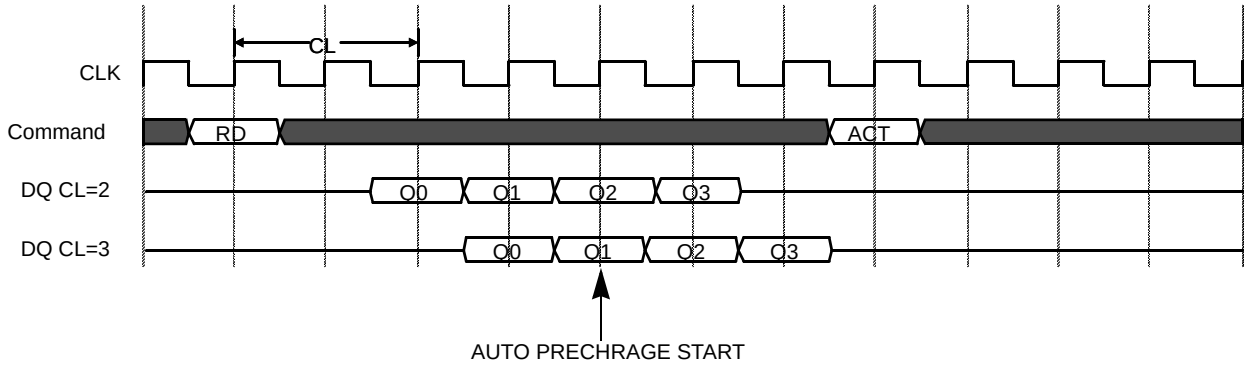
BL=4

Note 1. tDPL should be required to excute precharge after burst write. tDPL = 1 CLK for $\overline{CAS}$ latency 2 and 3

AUTO PRECHARGE

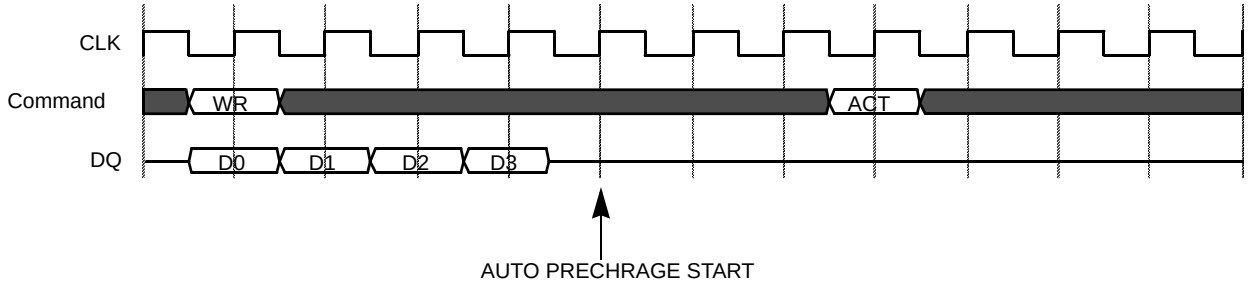
This command is used to precharge active bank without precharge command during the read and write cycle. A read (or write) and precharge cycle are performed within minimun tRAS cycle. The auto precharge command is issued with read or write command at same clock rising edge. If read or write command is issued by asserting high on AP, then the bank will enter idle state after read or write cycle. A read or write command with auto precharge can not be terminated by read, write, precharge and burst stop. So these commands are prohibited during the read or write with auto precharge cycle.

BURST READ WITH AUTO PRECHARGE



BL=4, CL=2

BURST WRITE WITH AUTO PRECHARGE

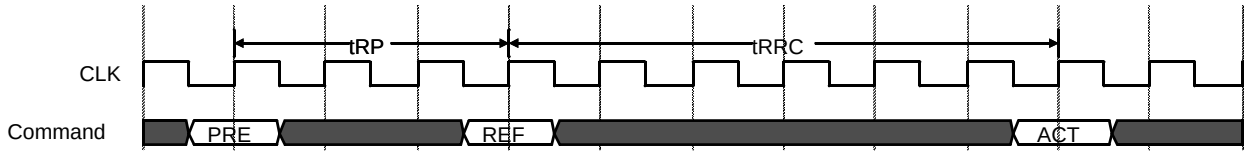


BL=4

AUTO REFRESH

This command is similar to $\overline{CAS}$ before $\overline{RAS}$ refresh command in asynchronous DRAMs. The auto refresh command is initiated by activating $\overline{CS}$, $\overline{CAS}$, $\overline{RAS}$ and deactivating $\overline{WE}$ at the same clock rising edge. One Auto Refresh cycle refreshes one row selected by on-chip refresh counter. The refresh counter is incremented during each Auto Refresh cycle. Because Auto Refresh operation alternate between banks, both banks must be idle when Auto Refresh commands are invoked. Once an Auto Refresh cycle has been invoked, it is controlled internally until its duration. NOP cycles must be inserted during the entire Auto Refresh cycle time defined by tRC cycle time. Since the SDRAM is a dynamic memory device, the stored data must be refreshed periodically or will be lost. To avoid data loss, all rows in both banks must be refreshed during the maximum refresh interval specified by tREF.

AUTO REFRESH



Note1

Note
1.All banks must be in idle state before excute auto refresh command. So Precharge command should be issued if necessary

SELF REFRESH

The SDRAM features an on-chip refresh cycle timing generator which can be used in conjunction with the row refresh counter to completely refresh the two banks of DRAM entirely under internal control. The self refresh entry command is initiated by asserting low on CKE and Auto Refresh command. Once this command is invoked, the cycle timing generator performs a burst refresh sequencing and CKE have to remains low to continue self refresh operation. Self Refresh can be invoked only when both banks are idle. While the device is in Self Refresh mode, CKE is the only enabled input to the device. All other inputs, including the clock are disabled and any input is ignored. Self refresh mode is exited by asserting high on CKE and system clock input. The low-to-high transition of CKE will re-enable the clock and other inputs asynchronously. A minimum time, specified by tSRE, must be required before any command. It is recommended that a burst of 4096 Auto Refresh commands be performed immediately after exiting Self Refresh mode.

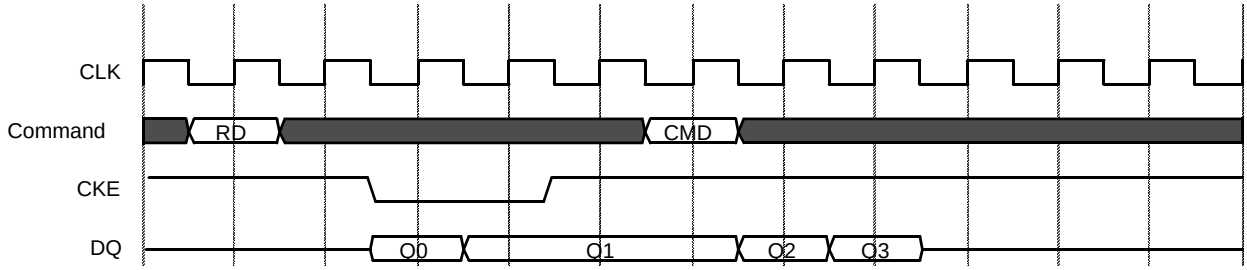
POWER DOWN

The SDRAM has two internal clock buffers. A low current capacity clock buffer feeds the CKE input buffer while a high current clock buffer feeds the state machine and all DRAM circuits. During the Power Down state, the large clock buffer is disabled but the small clock buffer is not. In contrast to the Self Refresh state, entering and exiting Power Down is completely synchronous with respect to CKE. That is, CKE is sampled on every clock cycle, rather than asynchronously changing the state of the SDRAM Power Down is the lowest power state available. During Power Down, the SDRAM is not refreshed. Therefore, the minimum refresh specification still applies during power down. Exiting Power Down requires one clock cycle, as shown in the figure. Other commands can be issued on the clock cycle following the Exit Power Down command cycle

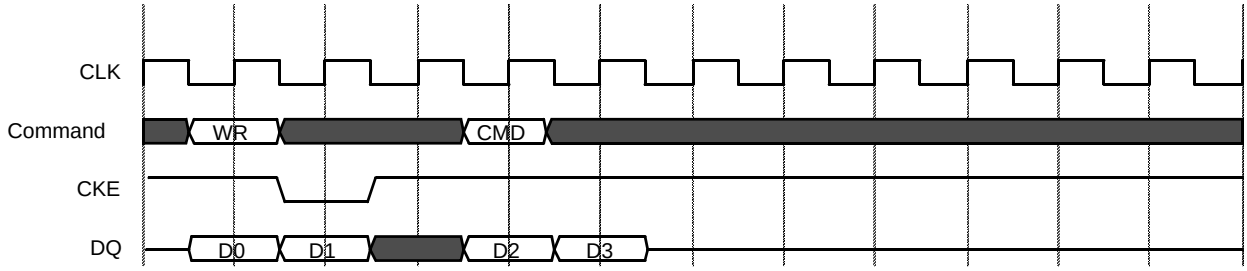
CLOCK SUSPEND

Clock Suspend is very similar to Power Down, except that the Clock Suspend command is invoked by sampling the CKE signal low while one or both banks are not idle. While the clock is suspended, only the CLK and CKE inputs are enabled, and the state of CKE is sampled on every clock cycle. Internally, the banks remain in the state they were in when the clock was suspended. For example, if bank 0 was in the middle of a read burst when the clock was suspended, the read state will be maintained after exiting Clock Suspend. On the next clock cycle, the burst can be resumed from the next memory location designated by the burst length and burst type programmed in the Mode Register, or other legal commands can be issued to the active or both banks. While the clock is suspended, the SDRAM is not refreshed. Therefore, the minimum refresh specification still applies during the period when the clock is suspended.

CLOCK SUSPEND DURING READ

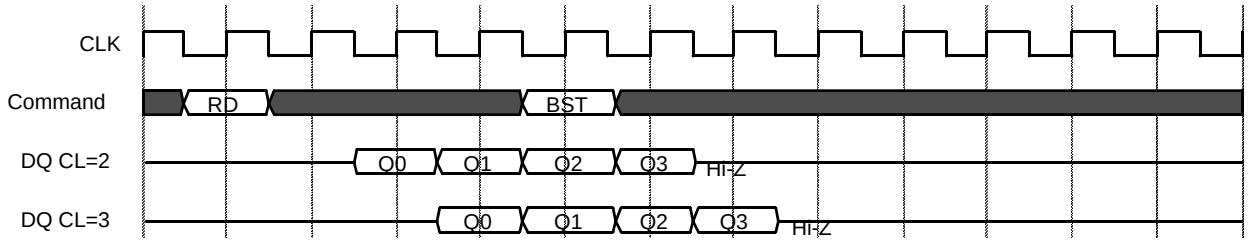


CLOCK SUSPEND DURING WRITE



BURST STOP

This command is used to terminate the burst operation during the read and write cycle. The burst stop command is initiated by activating $\overline{CS}$, $\overline{WE}$ and asserting high on $\overline{RAS}$ and High at the same clock rising edge. During the read cycle, read data is terminated and DQ pins go to Hi-Z after the $\overline{CAS}$ latency after the burst stop command. During the write cycle DQ pins go to Hi-Z at the same clock with the burst stop command.



STATE AND FUNCTIONAL TRUTH TABLE, OPERATIONS INVOLVING BOTH BANKS

Current State	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	AP	ADDR	Action
	Prev.	Curr.								
Power Down	L	L	X	X	X	X	X	X	X	Maintain Power Down
	L	H	L	H	H	H	X	X	X	Exit Power DownBBI
	L	H	H	X	X	X	X	X	X	Exit Power DownBBI
Self Refresh [1]	L	L	X	X	X	X	X	X	X	NOP(Maintain Self Refresh)
	H	L	L	L	L	H	X	X	X	Entry Self Refresh
	L	H	L	H	H	H	X	X	X	Exit Self Refresh
	L	H	H	X	X	X	X	X	X	
All Banks Idle(BBI)	H	L	L	H	H	H	X	X	X	Enter Power Down
	H	L	H	X	X	X	X	X	X	Enter Power Down
	H	L	L	L	L	H	X	X	X	Enter Self Refresh
	H	H	L	H	H	H	X	X	X	NOP
	H	H	H	X	X	X	X	X	X	Deselect
	H	H	L	L	L	L	OPCODE			Mode Register Access
	H	H	L	L	L	H	X	X	X	Auto Refresh
CLK Suspend	L	L	X	X	X	X	X	X	X	Maintain CLK Suspend
	L	H	X	X	X	X	X	X	X	Exit CLK Suspend
Auto Refresh	H	H	L	H	H	H	X	X	X	NOP All Banks Idle After tRC
	H	H	H	X	X	X	X	X	X	Deselect
Any state other than above	H	L	X	X	X	X	X	X	X	Suspend Clock, next Cycle Clock Suspend
DQM	H	X	X	X	X	X	X	X	X	Write DQM Latency is 0, Read DQM Latency is 2.

Note: 1. Exiting Self Refresh occurs by asynchronously bringing CKE from low to high.

STATE AND FUNCTIONAL TRUTH TABLE, SELECTED BANK

Current State of Selected Bank	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	AP	ADDR	Action to Selected Bank (Unless otherwise noted)
Idle	L	L	L	L	OPCODE			Mode Register Access
	L	H	H	H	X	X	X	NOP
	H	X	X	X	X	X	X	Deselect
	L	L	H	L	BA	X	X	NOP
	L	L	L	H	X	X	X	Auto or Self Refresh
	L	L	H	H	BA	RA	RA	Active Row
Row Active	L	L	L	X	X	X	X	ILLEGAL
	L	H	H	H	X	X	X	NOP
	H	X	X	X	X	X	X	Deselect
	L	L	H	L	BA	L	X	Precharge Selected Bank
	L	L	H	L	X	H	X	Precharge All Banks
	L	H	L	L	BA	L	CA	Begin Write
	L	H	L	L	BA	H	CA	Begin Write/Auto Precharge
	L	H	L	H	BA	L	CA	Begin Read
	L	H	L	H	BA	H	CA	Begin Read/Auto Precharge
Read	L	H	H	H	X	X	X	NOP(Continue burst to end Row Active)
	H	X	X	X	X	X	X	Deselect
	L	L	H	L	BA	L	X	Precharge Selected Bank
	L	L	H	L	X	H	X	Precharge All Banks
	L	L	L	X	X	X	X	ILLEGAL
	L	H	L	L	BA	L	CA	Begin Write [2]
	L	H	L	L	BA	H	CA	Begin Write/Auto Precharge [2]
	L	H	L	H	BA	L	CA	Begin New Read
	L	H	L	H	BA	H	CA	Begin New Read/Auto Precharge
	L	H	H	L	X	X	X	Term Burst Row Active
Write	L	H	H	H	X	X	X	NOP (Continue burst to end Row Active)
	H	X	X	X	X	X	X	Deselect
	L	L	H	L	BA	L	X	Precharge Selected Bank
	L	L	H	L	X	H	X	Precharge All Banks
	L	L	L	X	X	X	X	ILLEGAL
	L	H	L	L	BA	L	CA	Begin WRITE
	L	H	L	L	BA	H	CA	Begin Write/Auto Precharge
	L	H	L	H	BA	L	CA	Begin New Read
	L	H	L	H	BA	H	CA	Begin New Read/Auto Precharge
	L	H	H	L	X	X	X	Term Burst Row Active
Read with Atuo Precharging	L	H	H	H	X	X	X	NOP, Continue burst to end Pre-charge [3]
	H	X	X	X	X	X	X	Deselect
	L	L	H	L	BA	L	X	ILLEGAL
	L	L	H	L	X	H	X	ILLEGAL
	L	H	L	L	BA	L	CA	ILLEGAL
	L	H	L	L	BA	H	CA	ILLEGAL
	L	H	L	H	BA	L	CA	ILLEGAL
	L	H	L	H	BA	H	CA	ILLEGAL
	L	H	H	L	X	X	X	ILLEGAL
	L	L	L	X	X	X	X	ILLEGAL

Current State of Selected Bank	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	AP	ADDR	Action to Selected Bank (Unless otherwise noted)
Write with Auto Pre-charging	L	H	H	H	X	X	X	NOP, Continue burst to end Pre-charge [3]
	H	X	X	X	X	X	X	Deselect
	L	L	H	L	BA	L	X	ILLEGAL
	L	L	H	L	X	H	X	ILLEGAL
	L	H	L	L	BA	L	CA	ILLEGAL
	L	H	L	L	BA	H	CA	ILLEGAL
	L	H	L	H	BA	L	CA	ILLEGAL
	L	H	L	H	BA	H	CA	ILLEGAL
	L	H	H	L	X	X	X	ILLEGAL
	L	L	L	X	X	X	X	ILLEGAL
Precharging	L	H	H	H	X	X	X	NOP Idle after tRP
	H	X	X	X	X	X	X	Deselect
	L	L	H	L	BA	L	X	NOP
	L	L	H	L	X	H	X	NOP
	L	H	L	L	BA	L	CA	ILLEGAL
	L	H	L	L	BA	H	CA	ILLEGAL
	L	H	L	H	BA	L	CA	ILLEGAL
	L	H	L	H	BA	H	CA	ILLEGAL
	L	H	H	L	X	X	X	ILLEGAL
Row Activating	L	H	H	H	X	X	X	NOP
	H	X	X	X	X	X	X	Deselect
	L	L	H	L	BA	L	X	ILLEGAL
	L	L	H	L	X	H	X	ILLEGAL
	L	H	L	L	BA	X	CA	ILLEGAL
	L	H	L	H	BA	X	CA	ILLEGAL
	L	H	H	L	X	X	X	ILLEGAL
	L	L	L	X	X	X	X	ILLEGAL
Mode Register Accessing	L	H	H	H	X	X	X	NOP
	H	X	X	X	X	X	X	Deselect
	L	L	H	H	X	X	X	ILLEGAL
	L	L	L	H	X	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	H	H	L	X	X	X	ILLEGAL

Notes:

1. Assume CKE high on the previous and current clock cycles.
2. Read bust must terminate one cycle before the start of a write sequence. This can be accomplished in one of two ways. First, if the last bit of the burst is output two cycles before the start of the write sequencem the burst will terminate. And the output will tristate, the internal read pipeline will be flushed during the cycle before the write command is issued. Second, the burst can be terminated by bringing DQM high and issuing a terminate burst command two cycles before the write command. This will also quarantee that the output will tristate and the read pipeline will be flushed during the cycle before the write command is issued.
3 while either bank is executing a read or Write burst sequence with Auto Precharge selected, no Read or write commands are allowed to the opposite bank.
4. X=Do not care, L=Low, H=High, BA=Bank Address, RA= Row Address, CA=Column Address, Opcode=Operand Code, NOP=No Operatin Code, NOP=No Operation.

Address sequence for different burst lengths

Burst Length	Initial Address	Burst Type	
	A2A1A0	Sequential	Interleave
2	X X 0	0,1	0,1
	X X 1	1,0	1,0
4	X 0 0	0,1,2,3	0,1,2,3
	X 0 1	1,2,3,0	1,0,3,2
	X 1 0	2,3,0,1	2,3,0,1
	X 1 1	3,0,1,2	3,2,1,0
8	0 0 0	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7
	0 0 1	1,2,3,4,5,6,7,0	1,0,3,2,5,4,7,6
	0 1 0	2,3,4,5,6,7,0,1	2,3,0,1,6,7,4,5
	0 1 1	3,4,5,6,7,0,1,2	3,2,1,0,7,6,5,4
	1 0 0	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3
	1 0 1	5,6,7,0,1,2,3,4	5,4,7,6,1,0,3,2
	1 1 0	6,7,0,1,2,3,4,5	6,7,4,5,2,3,0,1
	1 1 1	7,0,1,2,3,4,5,6	7,6,5,4,3,2,1,0
Full page	Note	0,1,2,3,4,~~~,m 1,2,3,4,5,~~~,0 , , , m,0,1,2,3,~~~,m-1	Not supported

Note : 4Mx4 - Initial address : A9-A0, Page length : 1024, m=1023
2Mx8 - Initial address : A8-A0, Page length : 512, m= 511
1Mx16 - Initial address : A7-A0, Page length : 256, m= 255

PROGRAMMABLE MODE REGISTER

MODE REGISTER SET

A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	0	0	$\overline{\text{CAS}}$ Latency			BT	Burst Length		

A3	Burst Type
0	Sequential
1	Interleave

A6	A5	A4	$\overline{\text{CAS}}$ Latency
0	0	0	Reserved
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

A2	A1	A0	Burst Length
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Full Page

Note: 1. Full page burst supports only sequential type

TEST MODE

A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address
X	X	X	X	X	X	1	X	X	X	X	X	X	X	Refresh Counter Test

Note: Test Mode - Used to test the counter of Auto Refresh
- Exit test mode using 'Precharge All bank'.