DDR SDRAM Device Operation

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OPERATION COMMAND TRUTH TABLE-I

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action
IDLE	H	X	X	X	X	DSEL	NOP or power down[3]
	L	H	H	H	X	NOP	NOP or power down[3]
	L	H	H	L	X	BST	ILLEGAL[4]
	L	H	L	H	BA, CA, AP	READ/READAP	ILLEGAL[4]
	L	H	L	L	BA, CA, AP	WRITE/WRITEAP	ILLEGAL[4]
	L	L	H	H	BA, RA	ACT	Row Activation
	L	L	H	L	BA, AP	PRE/PALL	NOP
	L	L	L	H	X	AREF/SREF	Auto Refresh or Self Refresh[5]
	L	L	L	L	OPCODE	MRS	Mode Register Set
ROW ACTIVE	H	X	X	X	X	DSEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	BST	ILLEGAL[4]
	L	H	L	H	BA, CA, AP	READ/READAP	Begin read: optional AP[6]
	L	H	L	L	BA, CA, AP	WRITE/WRITEAP	Begin write: optional AP[6]
	L	L	H	H	BA, RA	ACT	ILLEGAL[4]
	L	L	H	L	BA, AP	PRE/PALL	Precharge[7]
	L	L	L	H	X	AREF/SREF	ILLEGAL[11]
	L	L	L	L	OPCODE	MRS	ILLEGAL[11]
READ	H	X	X	X	X	DSEL	Continue burst to end
	L	H	H	H	X	NOP	Continue burst to end
	L	H	H	L	X	BST	Terminate burst
	L	H	L	H	BA, CA, AP	READ/READAP	Term burst, new read:optional AP[8]
	L	H	L	L	BA, CA, AP	WRITE/WRITEAP	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL[4]
	L	L	H	L	BA, AP	PRE/PALL	Term burst, precharge
	L	L	L	H	X	AREF/SREF	ILLEGAL[11]
	L	L	L	L	OPCODE	MRS	ILLEGAL[11]
WRITE	H	X	X	X	X	DSEL	Continue burst to end
	L	H	H	H	X	NOP	Continue burst to end
	L	H	H	L	X	BST	ILLEGAL[4]
	L	H	L	H	BA, CA, AP	READ/READAP	Term burst, new read:optional AP[8]
	L	H	L	L	BA, CA, AP	WRITE/WRITEAP	Term burst, new write:optional AP

OPERATION COMMAND TRUTH TABLE-II

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action
WRITE	L	L	H	H	BA, RA	ACT	ILLEGAL[4]
	L	L	H	L	BA, AP	PRE/PALL	Term burst, precharge
	L	L	L	H	X	AREF/SREF	ILLEGAL[11]
	L	L	L	L	OPCODE	MRS	ILLEGAL[11]
READ WITH AUTOPRE-CHARGE[12]	H	X	X	X	X	DSEL	Continue burst to end
	L	H	H	H	X	NOP	Continue burst to end
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, AP	READ/READAP	ILLEGAL[10]
	L	H	L	L	BA, CA, AP	WRITE/WRITEAP	ILLEGAL[10]
	L	L	H	H	BA, RA	ACT	ILLEGAL[4,10]
	L	L	H	L	BA, AP	PRE/PALL	ILLEGAL[4,10]
	L	L	L	H	X	AREF/SREF	ILLEGAL[11]
	L	L	L	L	OPCODE	MRS	ILLEGAL[11]
WRITE WITH AUTOPRE-CHARGE[13]	H	X	X	X	X	DSEL	Continue burst to end
	L	H	H	H	X	NOP	Continue burst to end
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, AP	READ/READAP	ILLEGAL[10]
	L	H	L	L	BA, CA, AP	WRITE/WRITEAP	ILLEGAL[10]
	L	L	H	H	BA, RA	ACT	ILLEGAL[4,10]
	L	L	H	L	BA, AP	PRE/PALL	ILLEGAL[4,10]
	L	L	L	H	X	AREF/SREF	ILLEGAL[11]
	L	L	L	L	OPCODE	MRS	ILLEGAL[11]
PRE-CHARGE	H	X	X	X	X	DSEL	NOP-Enter IDLE after tRP
	L	H	H	H	X	NOP	NOP-Enter IDLE after tRP
	L	H	H	L	X	BST	ILLEGAL[4]
	L	H	L	H	BA, CA, AP	READ/READAP	ILLEGAL[4,10]
	L	H	L	L	BA, CA, AP	WRITE/WRITEAP	ILLEGAL[4,10]
	L	L	H	H	BA, RA	ACT	ILLEGAL[4,10]
	L	L	H	L	BA, AP	PRE/PALL	NOP-Enter IDLE after tRP
	L	L	L	H	X	AREF/SREF	ILLEGAL[11]
	L	L	L	L	OPCODE	MRS	ILLEGAL[11]

OPERATION COMMAND TRUTH TABLE-III

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action
ROW ACTIVATING	H	X	X	X	X	DSEL	NOP - Enter ROW ACT after tRCD
	L	H	H	H	X	NOP	NOP - Enter ROW ACT after tRCD
	L	H	H	L	X	BST	ILLEGAL[4]
	L	H	L	H	BA, CA, AP	READ/READAP	ILLEGAL[4,10]
	L	H	L	L	BA, CA, AP	WRITE/WRITEAP	ILLEGAL[4,10]
	L	L	H	H	BA, RA	ACT	ILLEGAL[4,9,10]
	L	L	H	L	BA, AP	PRE/PALL	ILLEGAL[4,10]
	L	L	L	H	X	AREF/SREF	ILLEGAL[11]
	L	L	L	L	OPCODE	MRS	ILLEGAL[11]
WRITE RECOVERING	H	X	X	X	X	DSEL	NOP - Enter ROW ACT after tWR
	L	H	H	H	X	NOP	NOP - Enter ROW ACT after tWR
	L	H	H	L	X	BST	ILLEGAL[4]
	L	H	L	H	BA, CA, AP	READ/READAP	ILLEGAL
	L	H	L	L	BA, CA, AP	WRITE/WRITEAP	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL[4,10]
	L	L	H	L	BA, AP	PRE/PALL	ILLEGAL[4,11]
	L	L	L	H	X	AREF/SREF	ILLEGAL[11]
	L	L	L	L	OPCODE	MRS	ILLEGAL[11]
WRITE RECOVERING WITH AUTOPRE-CHARGE	H	X	X	X	X	DSEL	NOP - Enter precharge after tWR
	L	H	H	H	X	NOP	NOP - Enter precharge after tWR
	L	H	H	L	X	BST	ILLEGAL[4]
	L	H	L	H	BA, CA, AP	READ/READAP	ILLEGAL[4,8,10]
	L	H	L	L	BA, CA, AP	WRITE/WRITEAP	ILLEGAL[4,10]
	L	L	H	H	BA, RA	ACT	ILLEGAL[4,10]
	L	L	H	L	BA, AP	PRE/PALL	ILLEGAL[4,11]
	L	L	L	H	X	AREF/SREF	ILLEGAL[11]
	L	L	L	L	OPCODE	MRS	ILLEGAL[11]
REFRESHING	H	X	X	X	X	DSEL	NOP - Enter IDLE after tRC
	L	H	H	H	X	NOP	NOP - Enter IDLE after tRC
	L	H	H	L	X	BST	ILLEGAL[11]
	L	H	L	H	BA, CA, AP	READ/READAP	ILLEGAL[11]

OPERATION COMMAND TRUTH TABLE-IV

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action
MODE REGISTER ACCESSING	H	X	X	X	X	DSEL	NOP - Enter IDLE after tMRD
	L	H	H	H	X	NOP	NOP - Enter IDLE after tMRD
	L	H	H	L	X	BST	ILLEGAL[11]
	L	H	L	H	BA, CA, AP	READ/READAP	ILLEGAL[11]
	L	H	L	L	BA, CA, AP	WRITE/WRITEAP	ILLEGAL[11]
	L	L	H	H	BA, RA	ACT	ILLEGAL[11]
	L	L	H	L	BA, AP	PRE/PALL	ILLEGAL[11]
	L	L	L	H	X	AREF/SREF	ILLEGAL[11]
	L	L	L	L	OPCODE	MRS	ILLEGAL[11]

Note:

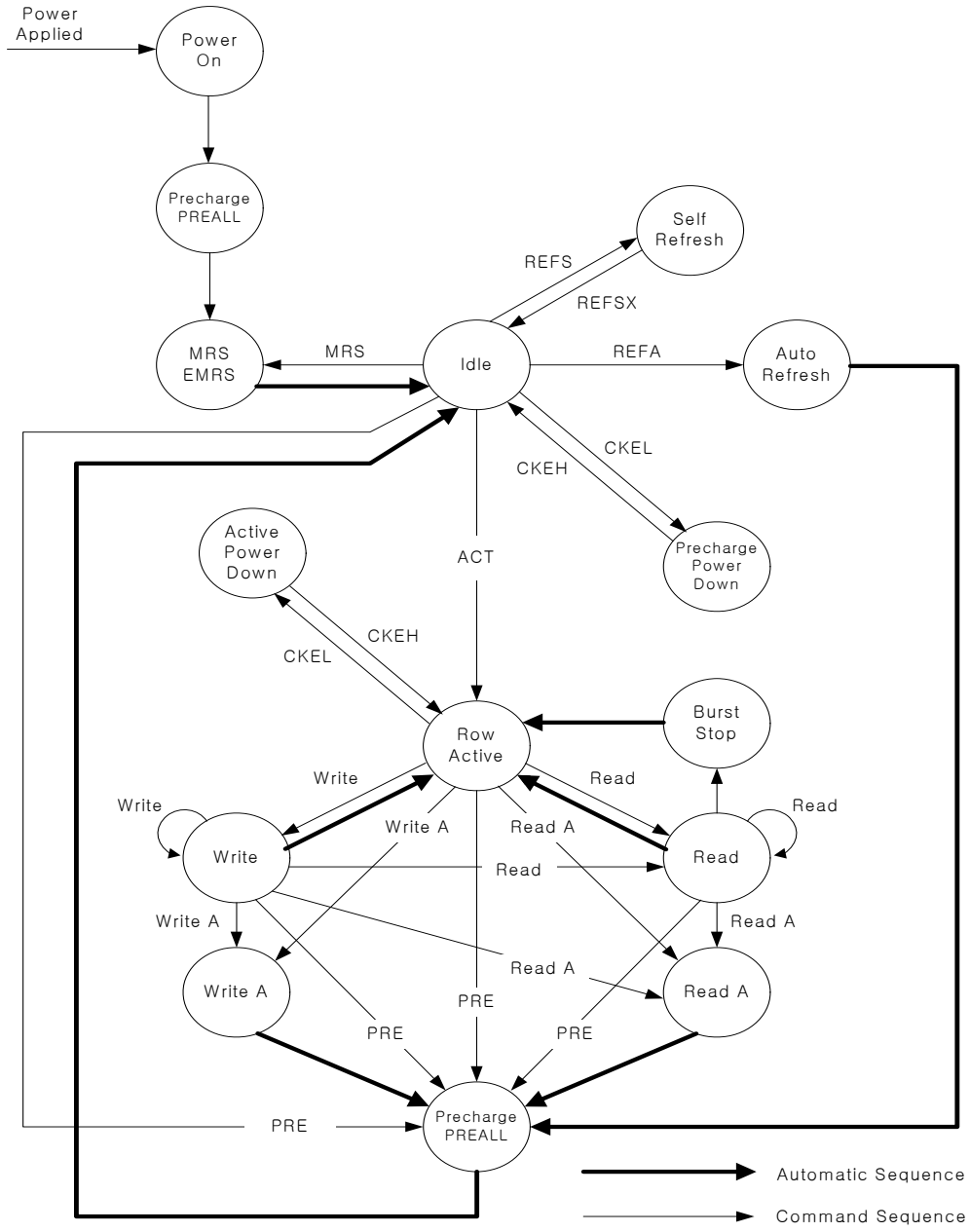
1. H - Logic High Level, L - Logic Low Level, X - Don't Care, V - Valid Data Input, BA - Bank Address, AP - AutoPrecharge Address, CA - Column Address, RA - Row Address, NOP - NO Operation.
2. All entries assume that CKE was active(high level) during the preceding clock cycle.
3. If both banks are idle and CKE is inactive(low level), then in power down mode.
4. Illegal to bank in specified state. Function may be legal in the bank indicated by Bank Address(BA) depending on the state of that bank.
5. If both banks are idle and CKE is inactive(low level), then self refresh mode.
6. Illegal if tRCD is not met.
7. Illegal if tRAS is not met.
8. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
9. Illegal if tRRD is not met.
10. Illegal for single bank, but legal for other banks in multi-bank devices.
11. Illegal for all banks.
12. Refer to "Burst Read with Auto Precharge" in Device Operation for detail information
13. Refer to "Burst Write with Auto Precharge" in Device Operation for detail information

CKE FUNCTION TRUTH TABLE

Current State	CKEn-1	CKEn	/CS	/RAS	/CAS	/WE	/ADD	Action
SELF REFRESH[1]	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit self refresh, enter idle after tSREX
	L	H	L	H	H	H	X	Exit self refresh, enter idle after tSREX
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP, continue self refresh
POWER DOWN[2]	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit power down, enter idle
	L	H	L	H	H	H	X	Exit power down, enter idle
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP, continue power down mode
ALL BANKS IDLE[4]	H	H	X	X	X	X	X	See operation command truth table
	H	L	L	L	L	H	X	Enter self refresh
	H	L	H	X	X	X	X	Exit power down
	H	L	L	H	H	H	X	Exit power down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	H	X	X	ILLEGAL
	H	L	L	L	L	L	X	ILLEGAL
	L	L	X	X	X	X	X	NOP
ANY STATE OTHER THAN ABOVE	H	H	X	X	X	X	X	See operation command truth table
	H	L	X	X	X	X	X	ILLEGAL[5]
	L	H	X	X	X	X	X	INVALID
	L	L	X	X	X	X	X	INVALID

Note:
When CKE=L, all DQ and DQS must be in Hi-Z state.
1. CKE and /CS must be kept high for a minimum of 200 stable input clocks before issuing Read command. (See the parameter 'Exit Self Refresh to non-Read command' in AC CHARACTERISTICS for non-Read command)
2. All command can be stored after 2 clocks from low to high transition of CKE.
3. Illegal if CK is suspended or stopped during the power down mode.
4. Self refresh can be entered only from the all banks idle state.
5. Disabling CK may cause malfunction of any bank which is in active state.

SIMPLIFIED STATE DIAGRAM



PREALL = Precharge All Banks
MRS = Mode Register Set
EMRS = Extended Mode Register Set
REFS = Enter Self Refresh
REFSX = Exit Self Refresh
REFA = Auto Refresh

CKEL = Enter Power Down
CKEH = Exit Power Down
ACT = Active
Write A = Write with Autoprecharge
Read A = Read with Autoprecharge
PRE = Precharge

POWER-UP SEQUENCE AND DEVICE INITIALIZATION

DDR SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Power must first be applied to VDD, then to VDDQ, and finally to VREF (and to the system VTT). VTT must be applied after VDDQ to avoid device latch-up, which may cause permanent damage to the device. VREF can be applied anytime after VDDQ, but is expected to be nominally coincident with VTT. Except for CKE, inputs are not recognized as valid until after VREF is applied. CKE is an SSTL_2 input, but will detect an LVCMOS LOW level after VDD is applied. Maintaining an LVCMOS LOW level on CKE during power-up is required to guarantee that the DQ and DQS outputs will be in the High-Z state, where they will remain until driven in normal operation (by a read access). After all power supply and reference voltages are stable, and the clock is stable, the DDR SDRAM requires a 200us delay prior to applying an executable command.

Once the 200us delay has been satisfied, a DESELECT or NOP command should be applied, and CKE should be brought HIGH. Following the NOP command, a PRECHARGE ALL command should be applied. Next a EXTENDED MODE REGISTER SET command should be issued for the Extended Mode Register, to enable the DLL, then a MODE REGISTER SET command should be issued for the Mode Register, to reset the DLL, and to program the operating parameters. After the DLL reset, tXSRD(DLL locking time) should be satisfied for read command. After the Mode Register set command, a PRECHARGE ALL command should be applied, placing the device in the all banks idle state.

Once in the idle state, two AUTO REFRESH cycles must be performed. Additionally, a MODE REGISTER SET command for the Mode Register with the reset DLL bit deactivated (i.e. to program operating parameters without resetting the DLL) must be performed. Following these cycles, the DDR SDRAM is ready for normal operation.

1. Apply power - VDD, VDDQ, VTT, VREF in the following power up sequencing and attempt to maintain CKE at LVCMOS low state. (All the other input pins may be undefined.)

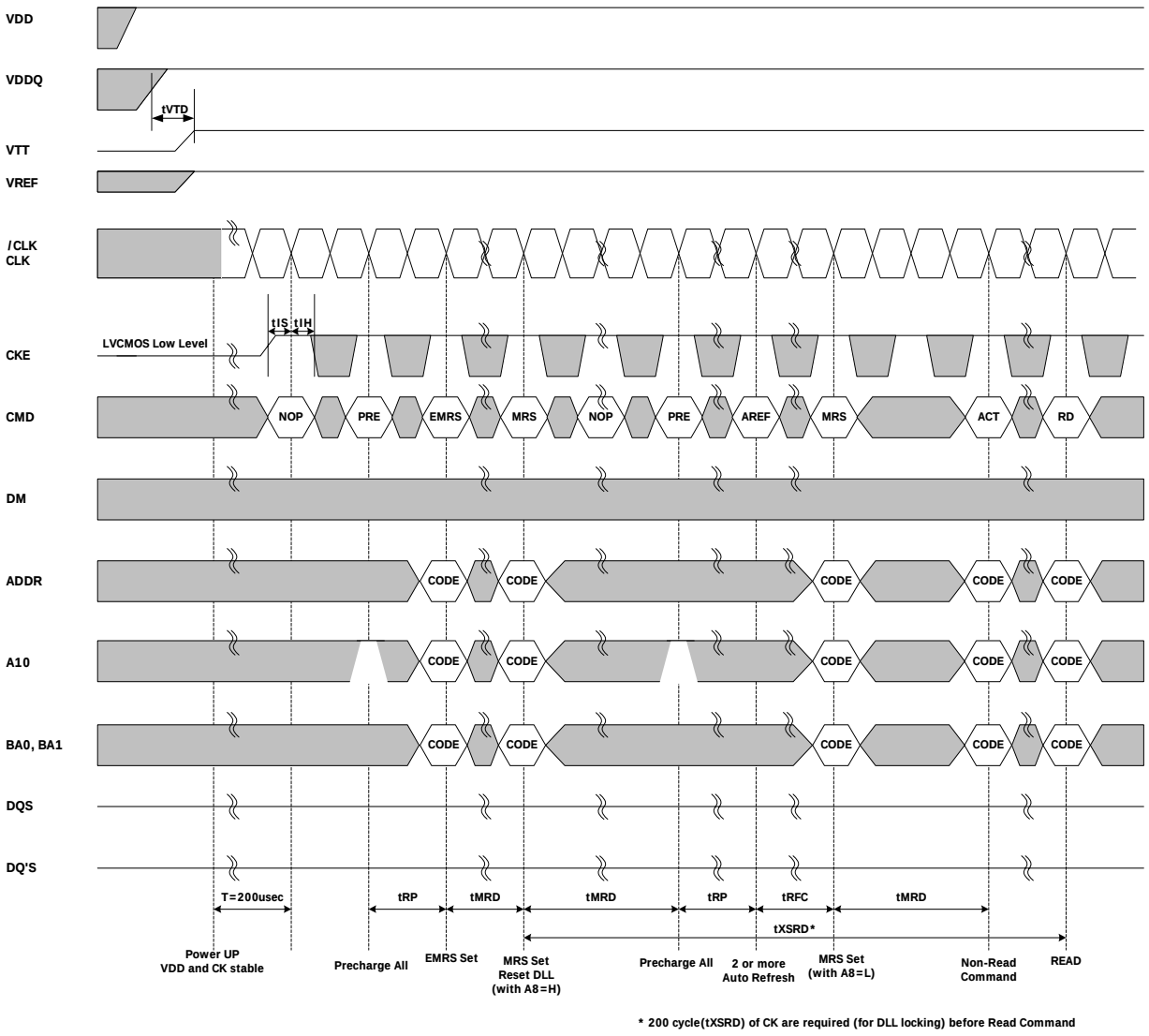
   - VDD and VDDQ are driven from a single power converter output.
   - VTT is limited to 1.44V (reflecting VDDQ(max)/2 + 50mV VREF variation + 40mV VTT variation.
   - VREF tracks VDDQ/2.
   - A minimum resistance of 42 Ohms (22 ohm series resistor + 22 ohm parallel resistor - 5% tolerance) limits the input current from the VTT supply into any pin.
   - If the above criteria cannot be met by the system design, then the following sequencing and voltage relationship must be adhered to during power up.

Voltage description	Sequencing	Voltage relationship to avoid latch-up
VDDQ	After or with VDD	< VDD + 0.3V
VTT	After or with VDDQ	< VDDQ + 0.3V
VREF	After or with VDDQ	< VDDQ + 0.3V

2. Start clock and maintain stable clock for a minimum of 200usec.
3. After stable power and clock, apply NOP condition and take CKE high.
4. Issue Extended Mode Register Set (EMRS) to enable DLL.
5. Issue Mode Register Set (MRS) to reset DLL and set device to idle state with bit A8=High. (An additional 200 cycles of clock are required for locking DLL)
6. Issue Precharge commands for all banks of the device.

7. Issue 2 or more Auto Refresh commands.
8. Issue a Mode Register Set command to initialize the mode register with bit A8 = Low.

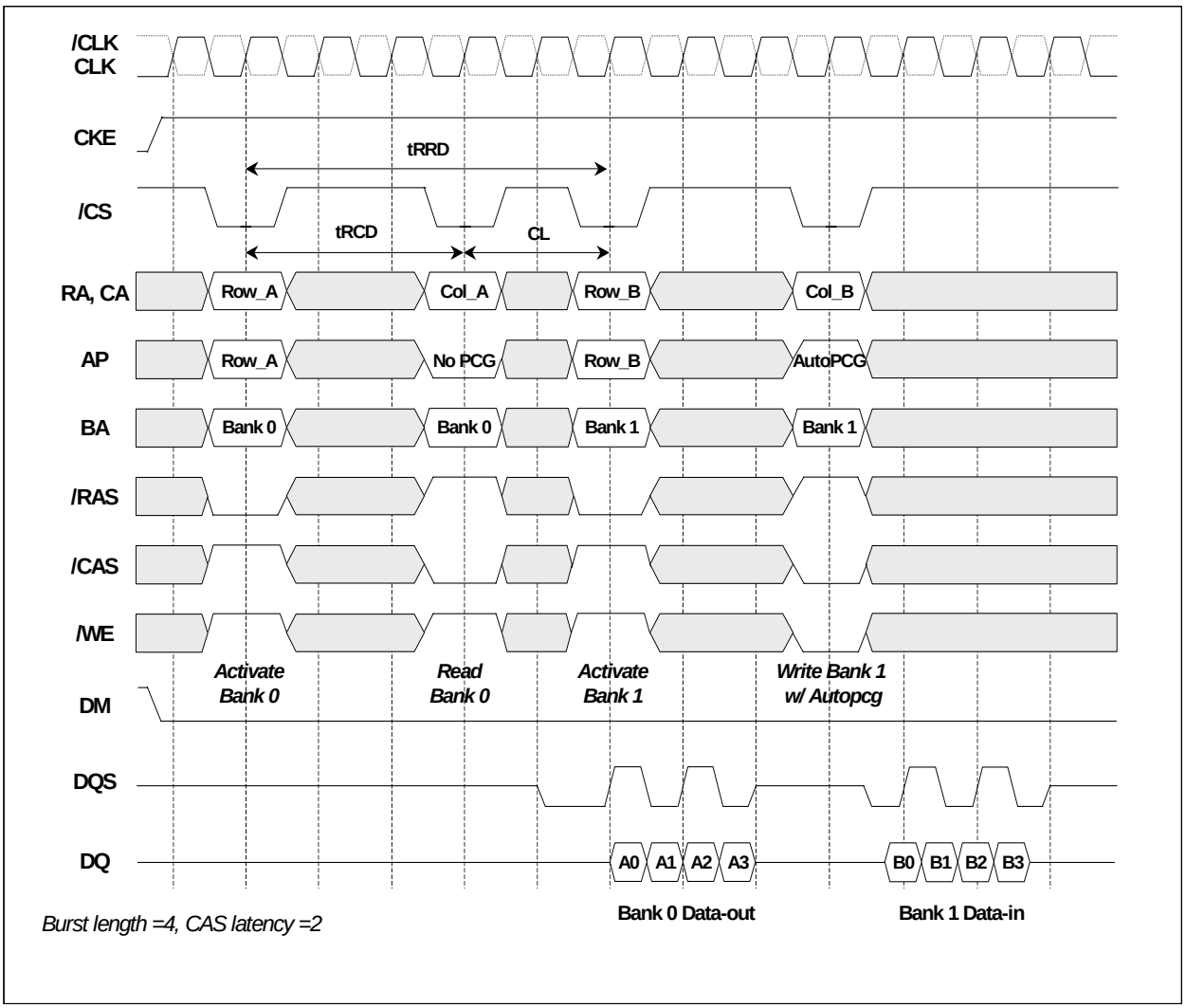
Power-Up Sequence



Burst Read and Burst Write

Burst Read and Burst Write commands are initiated as listed in Fig.1. Before the Burst Read command, the bank must be activated earlier. After /RAS to /CAS delay (tRCD), read operation starts. DDR SDRAM has been implemented with Data Strobe signal (DQS) which toggles high and low during burst with the same frequency as clock (CLK, /CLK). After CAS Latency (CL) which is defined as the interval between command clock and the first rising edge of the DQS, read data is launched onto data pin (DQ) with reference to DQS signal edge. Burst Write command in another bank can be given with having activated that bank where /RAS to /RAS delay (tRRD) is satisfied. Write data is also referenced and aligned to the DQS signal sent from the memory controller. Since all read operation bursts data out at both the rising and the falling of the DQS, double data bandwidth can be achieved, also for write data.

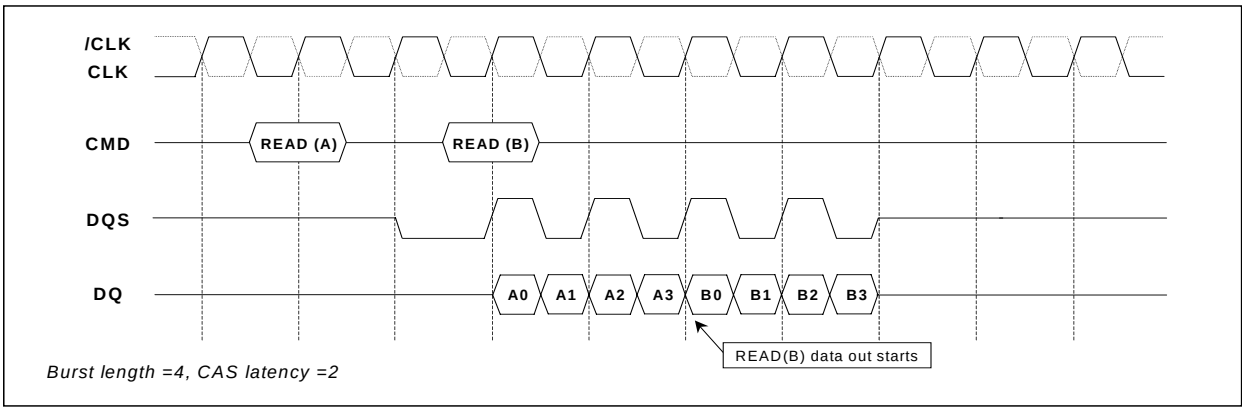
Fig.1. Burst Read and Burst Write



Burst Read followed by Burst Read

Back to back read operation in the same or different bank is possible as shown in Fig.2. Following first Read command, consecutive Read command can be initiated after BL/2 ticks of clock. In other words, minimum earliest possible Read command that does note interrupt the previous read data, can be issued after BL/2 clock is met. When Read(B) data out starts, data strobe signal does not transit to Hi-Z but toggle high and low for Read(B) data.

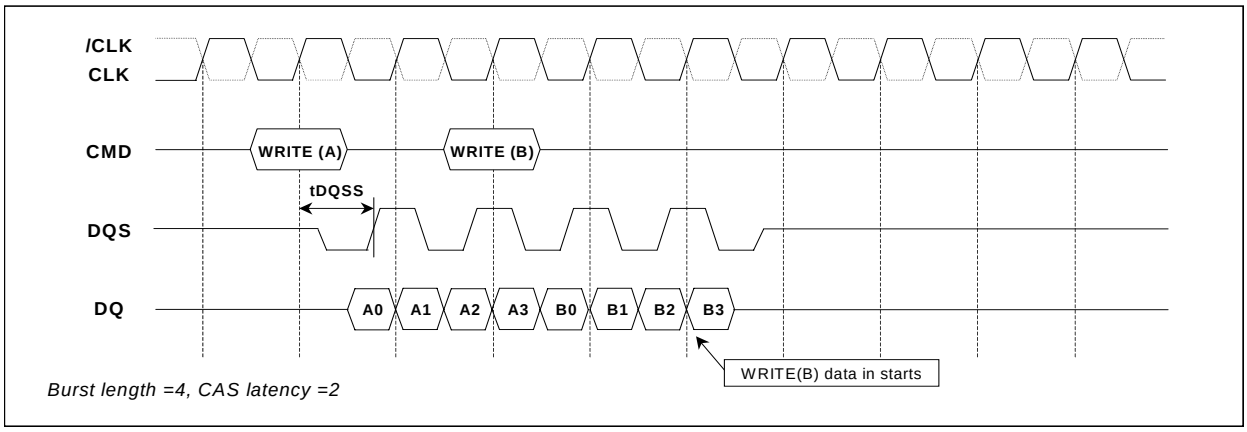
Fig.2. Burst Read followed by Burst Read



Burst Write followed by Burst Write

Back to back write operation in the same or different bank is possible as shown in Fig.3. Following first Write command, consecutive Write command can be initiated after BL/2 ticks of clock. In other words, minimum earliest possible Write command that does note interrupt the previous write data, can be issued after BL/2 clock is met. When Write(B) data in starts, data strobe signal does not transit to Hi-Z but toggle high and low for Write(B) data. Though the timing shown in Fig.3. is based on tDQSS=0.75*tCK, minimum number of clock of BL/2 for back to back write can be applied when tDQSS=1.25*tCK.

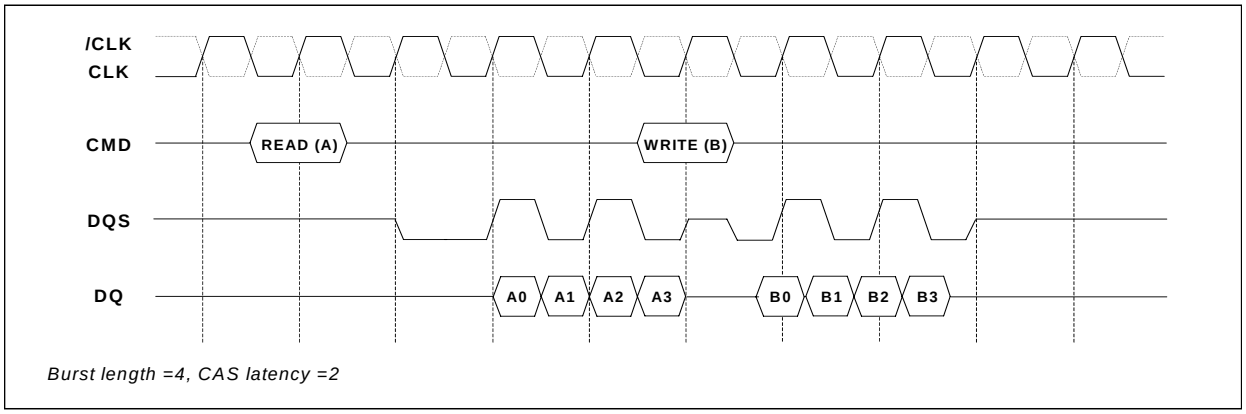
Fig.3. Burst Write followed by Burst Write



Burst Read followed by Burst Write

Back to back read followed by write operation in the same or different bank is possible as shown in Fig.4. Following first Read command, consecutive Write command can be initiated after RU{CL+BL/2} ticks of clock. (RU=Round Up for half cycle of CAS latency, such as 1.5 and 2.5). In other words, minimum earliest possible Write command that does not interrupt the previous read data can be issued after RU{CL+BL/2} clock is met.

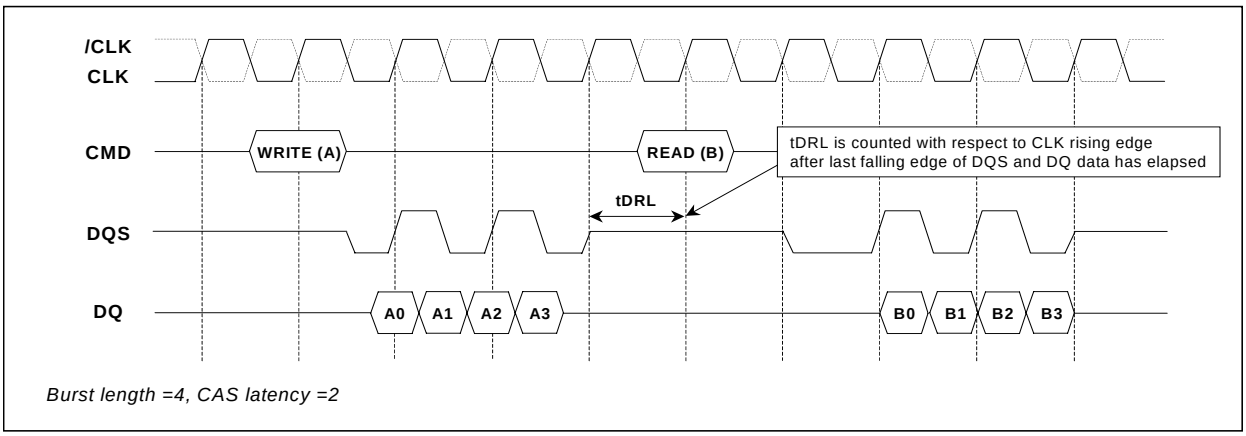
Fig.4. Burst Read followed by Burst Write



Burst Write followed by Burst Read

Back to back write followed by read operation in the same or different bank is possible as shown in Fig.5. Following first Write command, consecutive Read command can be initiated after (1+BL/2+tWTR) clock cycles. In other words, minimum earliest possible Read command that does not interrupt the previous write data can be issued after (1+BL/2+tWTR) clock is met.

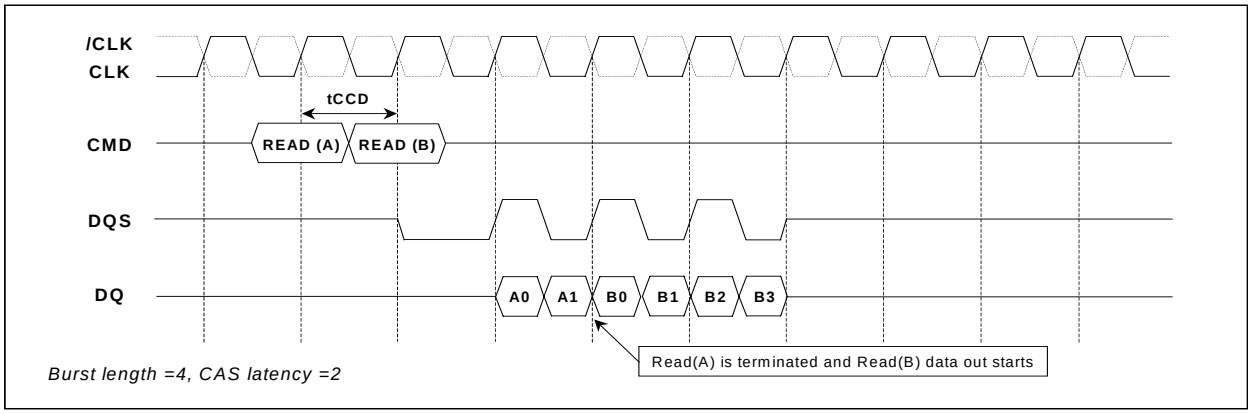
Fig.5. Burst Write followed by Burst Read



Burst Read terminated by another Burst Read

Read command terminates the previous Read command and the data is available after CAS latency for the new command. Minimum delay from a Read command to next Read command is determined by /CAS to /CAS delay (tCCD). Timing diagram is shown in Fig.6.

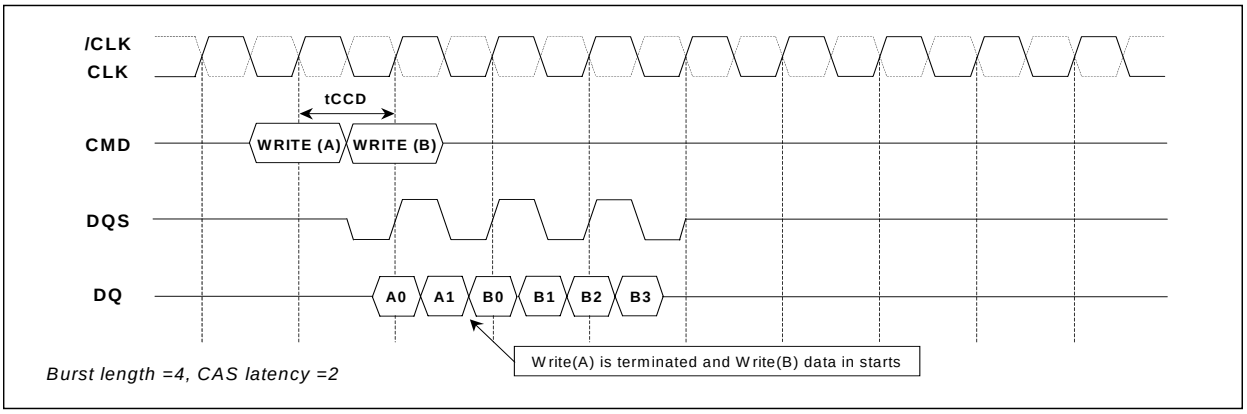
Fig.6. Burst Read terminated by another Burst Read



Burst Write terminated by another Burst Write

Write command terminates the previous Write command and the data is available after CAS latency for the new command. Fastest Write command to next Write command is determined by /CAS to /CAS delay (tCCD). Timing diagram is shown in Fig.7.

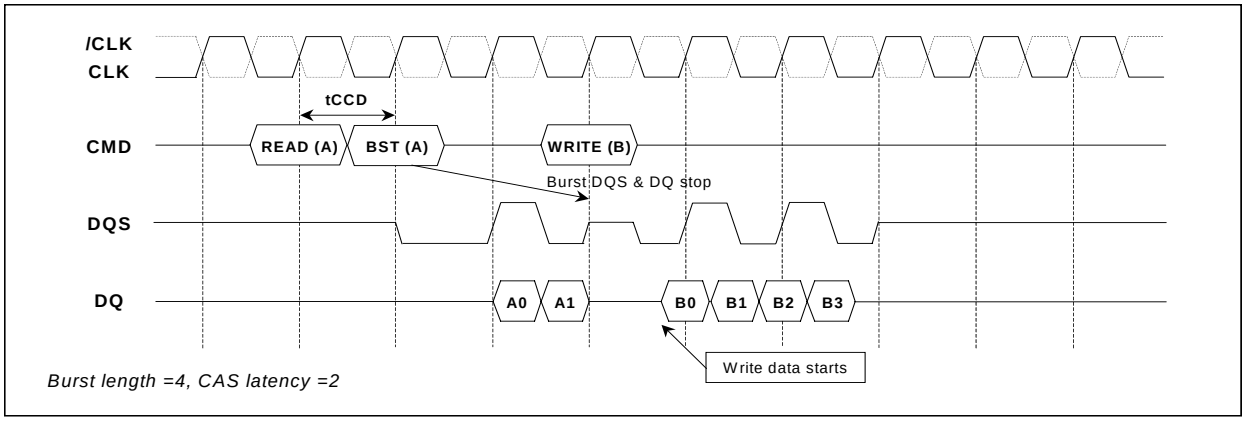
Fig.7. Burst Write terminated by another Burst Write



Burst Read terminated by another Burst Write

Write command terminates the previous Read command with the insertion of Burst Stop command that disables the previous Read command. The Burst Stop command interrupts bursting read data and data strobe signal with the same latency as CAS Latency (CL). The minimum delay for Write command after Burst Stop command is RU{CL} clocks irrespective BL. The Burst Stop command is valid for Read command only.

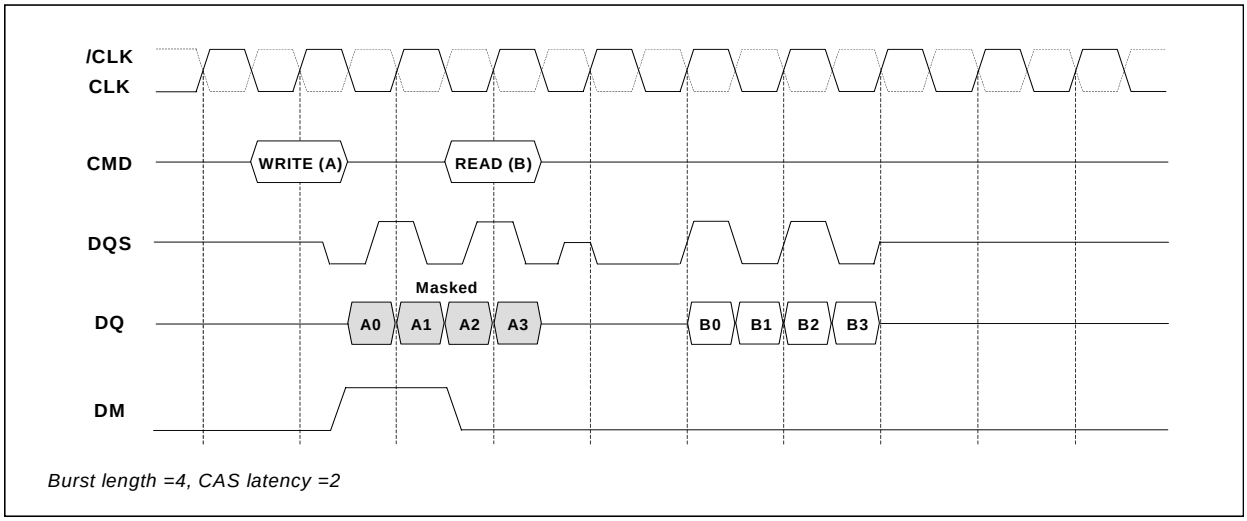
Fig.8. Burst Read terminated by another Burst Write



Burst Write terminated by another Burst Read

Read command terminates the previous Write command and the new burst read starts as shown in Fig.9. The minimum write to read command delay is 2 clock cycle irrespective of CL and BL. If input write data is masked by the Read command, DQ and DQS input are ignored by the DDR SDRAM. It is illegal for a Read command to interrupt a Write with autoprecharge command.

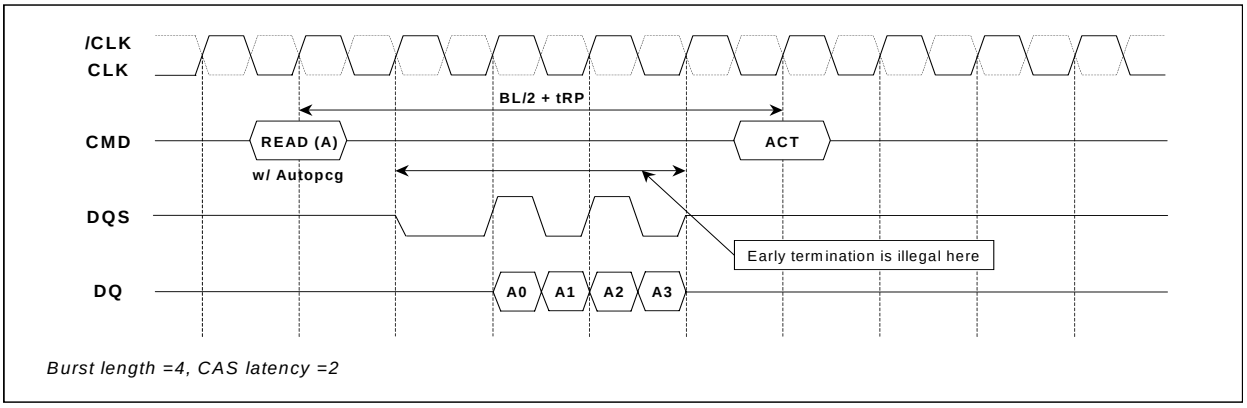
Fig.9. Burst Write terminated by another Burst Read



Burst Read with Auto Precharge

If a Read with Auto Precharge command is detected by memory component in CLK(n), then there will be no Active commands presented to this bank until CLK(n+BL/2+tRP). Internal precharging action will happen in CLK(n+BL/2).

Fig.10. Burst Read with Auto Precharge



When a Read with Auto Precharge command is issued, new command can be issued at each clock respectively as follows,

Issued command	For same bank			For different bank		
	CLK(n+1)	CLK(n+2)	CLK(n+3)	CLK(n+1)	CLK(n+2)	CLK(n+3)
READ	READ w/o AP	Illegal	Illegal	Legal	Legal	Legal
READ w/AP	READ w/ AP	Illegal	Illegal	Legal	Legal	Legal
ACTIVE	Illegal	Illegal	Illegal	Legal	Legal	Legal
PRECHARGE	Legal	Legal	Illegal	Legal	Legal	Legal

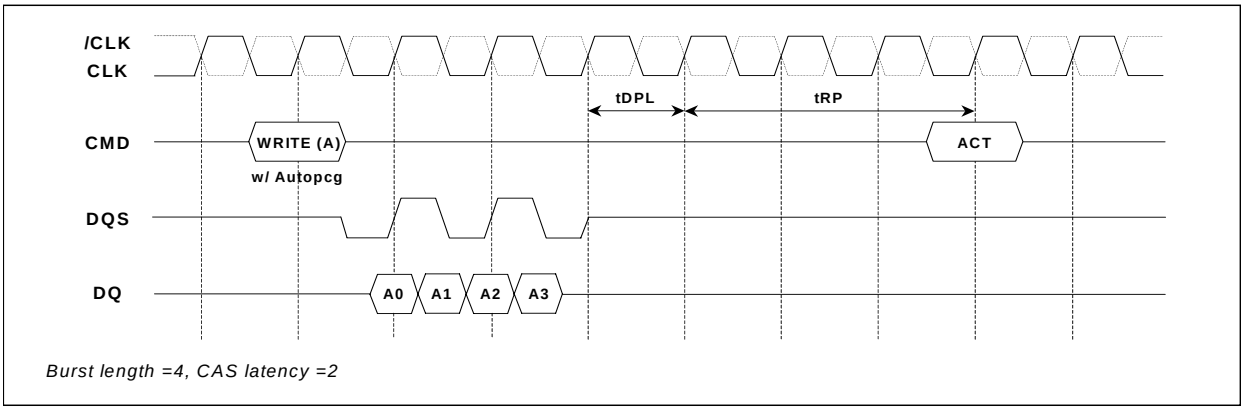
note:
1. WRITE(READ) w/ AP: WRITE(READ) with Auto Precharge
2. WRITE(READ) w/o AP: WRITE(READ) without Auto Precharge

Burst Write with Auto Precharge

If A10 is high when Write command is issued , the Write with Auto Precharge function is performed. Any new command to the same bank should not be issued until the internal precharge is completed. The internal precharge begins after keeping tWR(min).

tWR(Write Recovery Time) is referenced from the first positive CK edge after the last Data in pair.

Fig.12. Burst Write with Auto Precharge



When a Write with Auto Precharge command is issued, new command can be issued at each clock respectively as follows,

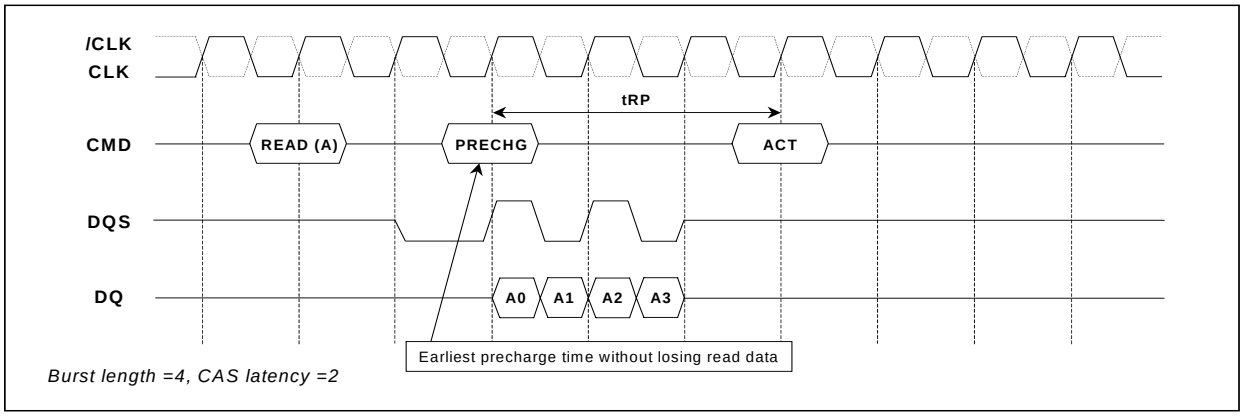
Issued command	For Same Bank						For Different Bank				
	CLK(n+1)	CLK(n+2)	CLK(n+3)	CLK(n+4)	CLK(n+5)	CLK(n+6)	CLK(n+1)	CLK(n+2)	CLK(n+3)	CLK(n+4)	CLK(n+5)
WRITE	WRITE w/o AP	WRITE w/o AP	Illegal	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal
WRITE w/AP	WRITE w/ AP	WRITE w/ AP	Illegal	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal
READ	Illegal	READ w/o AP+DM	READ w/o AP+DM	READ w/o AP	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal
READ w/AP	Illegal	READ w/ AP+DM	READ w/ AP+DM	READ w/ AP	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal
ACTIVE	Illegal	Illegal	Illegal	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal
PRECHARGE	Illegal	Illegal	Illegal	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal

note:
1. WRITE(READ) w/ AP: WRITE(READ) with Auto Precharge
2. WRITE(READ) w/o AP: WRITE(READ) without Auto Precharge

Precharge command after Burst Read

The earliest Precharge command can be issued after Read command without the loss of data is BL/2 clocks. The Precharge command can be given as soon as tRAS time is met. Fig.12 shows the earliest possible Precharge command can be issued for CL=2 and BL=4.

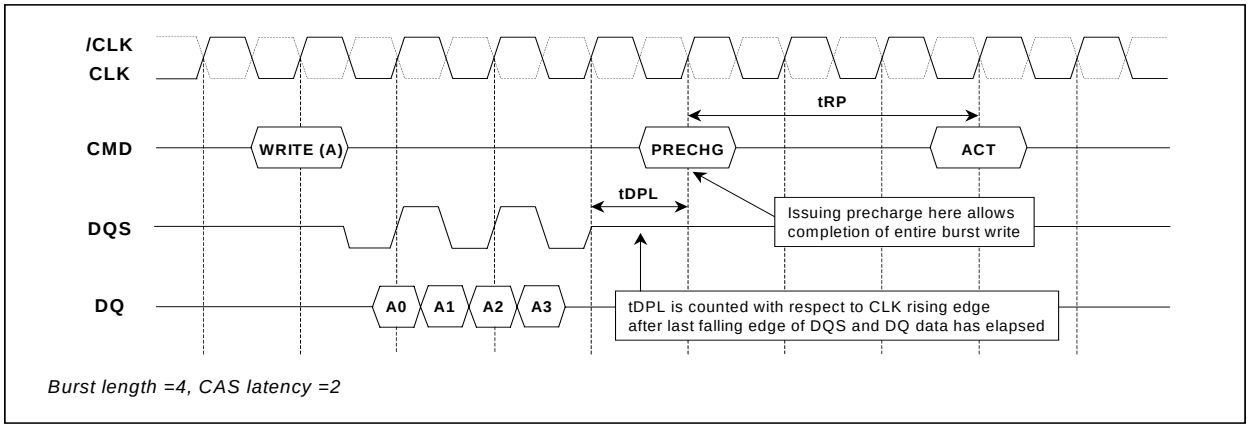
Fig.12. Precharge command after Burst Read



Precharge command after Burst Write

The earliest Precharge command can be issued after Write command without the loss of data is (BL/2+1+tWR) clock clycles. The Precharge command can be given as soon as tRAS time is met. Fig.13 shows the earliest possible Precharge command can be issued for CL=2 and BL=4.

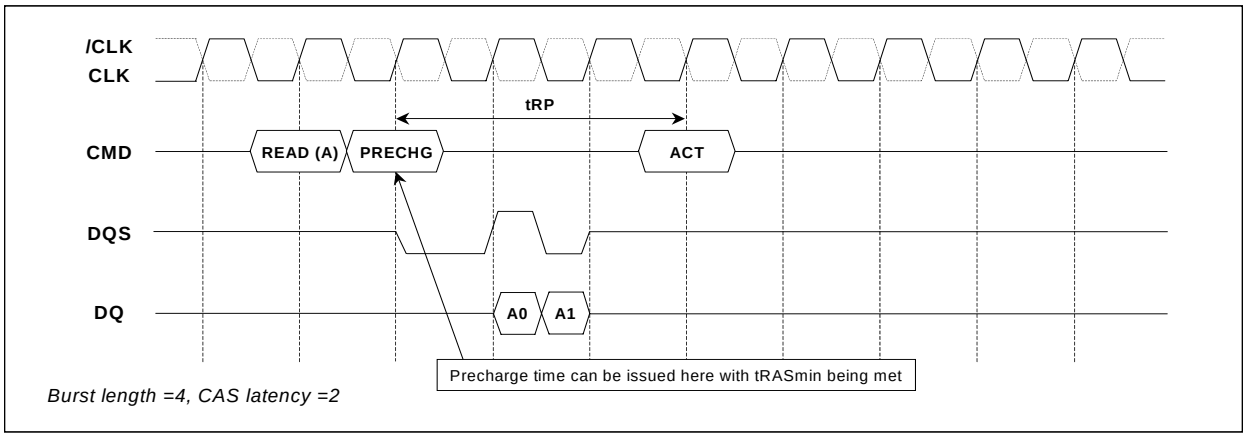
Fig.13. Precharge command after Burst Write



Precharge termination of Burst Read

The Burst Read (with no Autoprecharge) can be terminated earlier using a Precharge command as shown in Fig.14. This terminates read data when the remaining elements are not needed. It allows starting precharge early. The Precharge command can be issued any time after Burst Read command when tRAS time is met. Activation or other commands can be initiated after tRP time.

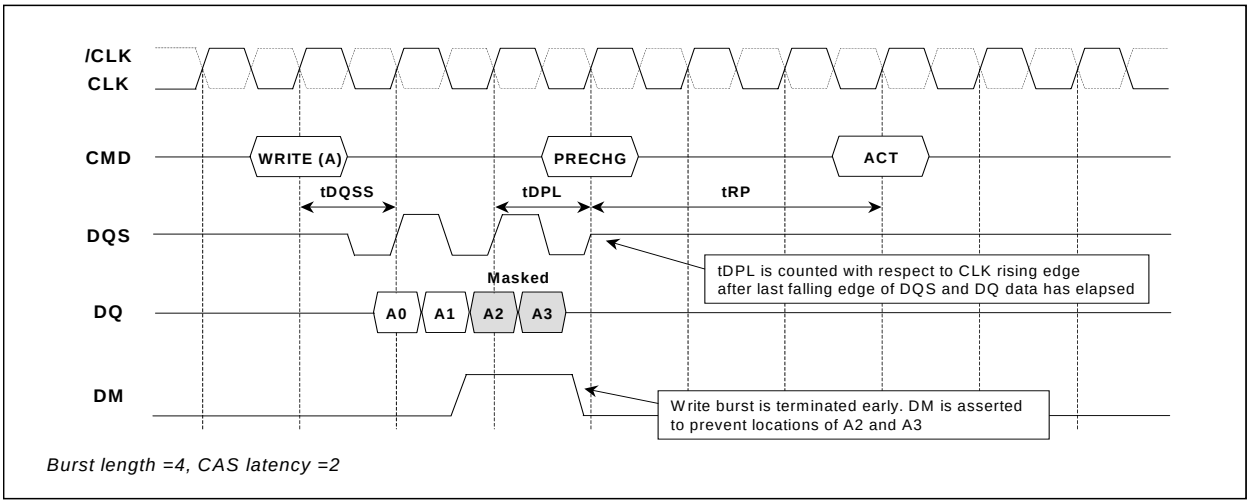
Fig.14. Precharge termination of Burst Read



Precharge termination of Burst Write

The Burst Write (with no Autoprecharge) can be terminated earlier using a Precharge command along with the Write Mask (DM) as shown in Fig.15. This terminates write data when the remaining elements are not needed. It allows starting precharge early. Precharge command can be issued after tWR(Write Recovery Time). DM should be used to mask the remaining data (A2 and A3 for this case). tRAS time must be met to issue the Precharge command.

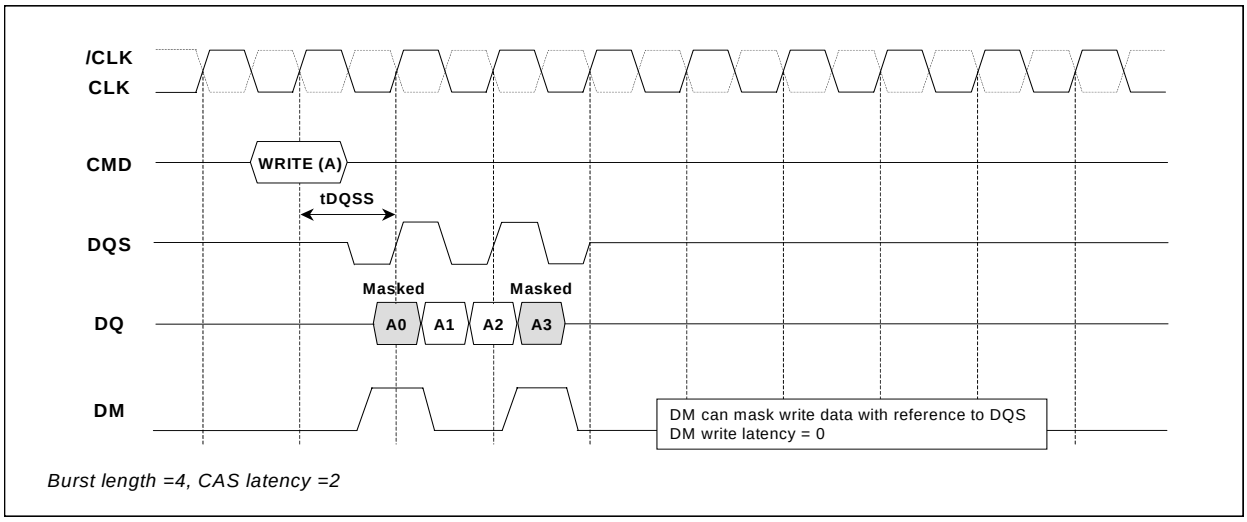
Fig.15. Precharge termination of Burst Write



DM masking (Write)

DM command masks burst write data with reference to data strobe signal and it is not related with read data. DM command can be initiated at both the rising edge and the falling edge of the DQS. DM latency for write operation is zero. For x16 data I/O, DDR SDRAM is equipped with LDM and UDM which control lower byte (DQ0~DQ7) and upper byte (DQ8~DQ15) respectively.

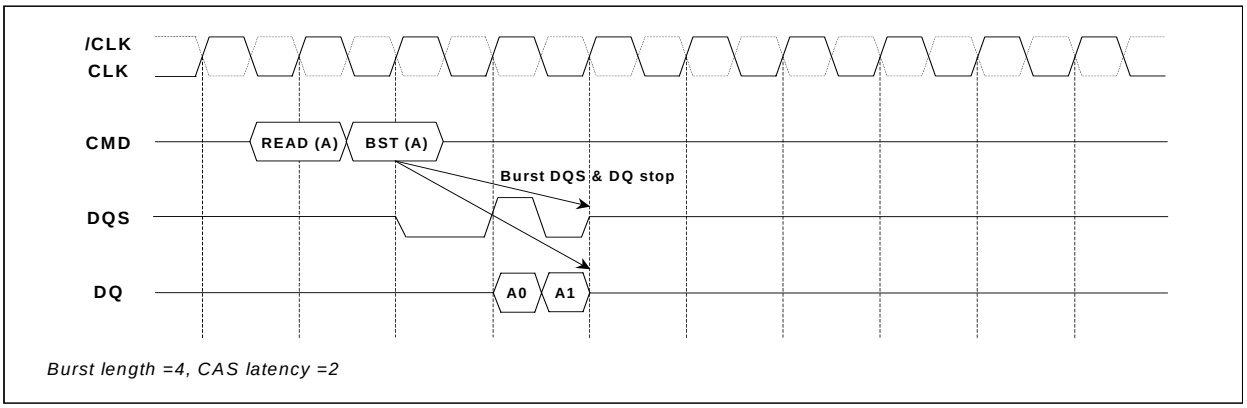
Fig.16. DM masking (Write)



Burst Stop command (Read)

When /CS=L, /RAS=H, /CAS=H and /WE=L, DDR SDRAM enter into Burst Stop mode, which bursts stop read data and data strobe signal with reference to clock signal. BST command can be initiated at the rising edge of the clock as other commands do. BST command is valid for read operation only. BST latency for read operation is the same as CL.

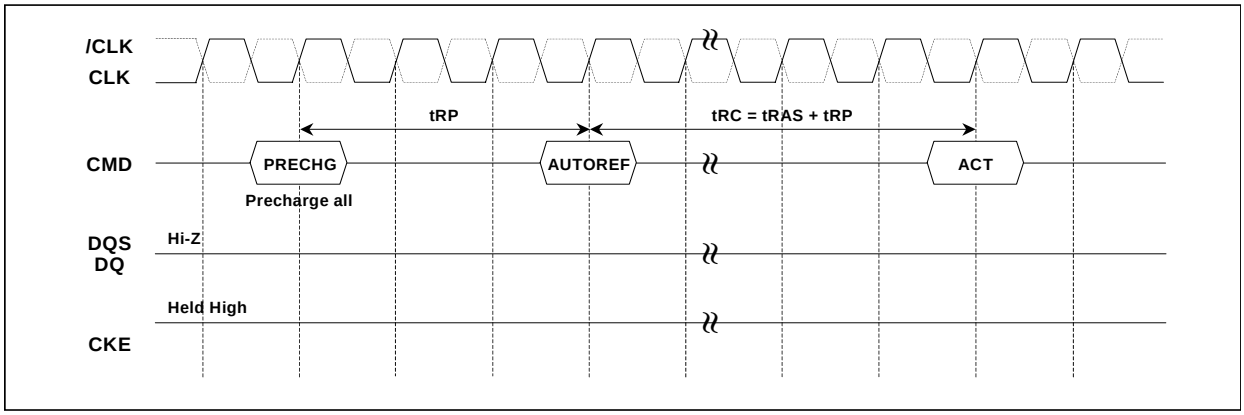
Fig.17. Burst Stop command (Read)



Auto Refresh and Precharge All command

When /CS=L, /RAS=L, /CAS=L and /WE=H, DDR SDRAM enter into Auto Refresh mode, which executes refresh operation with internal address increment. AREF command can be initiated at the rising edge of the clock as other commands do. Before entering Auto Refresh mode, all banks must be in a precharge state and AREF command can be issued after tRP period from Precharge All command.

Fig.18. Auto Refresh and Precharge All command

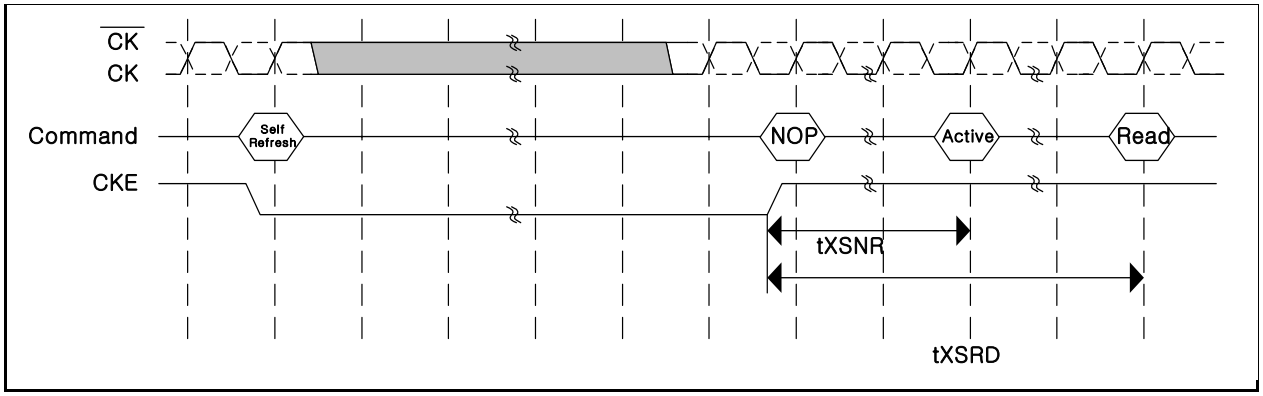


Self Refresh Entry and Exit

SELF REFRESH mode can be used when the device is in all bank idle state. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled(LOW). After entering SELF REFRESH mode, CKE must be held low to keep the device in self refresh mode. The DLL is automatically disabled upon entering SELF REFRESH, and is automatically enabled upon existing SELF REFRESH. Any time the DLL is enabled a DLL Reset must follow and 200 clock cycles should occur before a READ command can be issued. Input signals except CKE are "Don't Care" during SELF REFRESH.

The procedure for existing SELF REFRESH requires a sequence of commands. First, CK must be stable prior to CKE going back HIGH. Once CKE is HIGH, the DDR SDRAM must have NOP commands issued for tXSNR. Any non-read command can be issued after tXSNR and a read command can be issued after tXSRD.

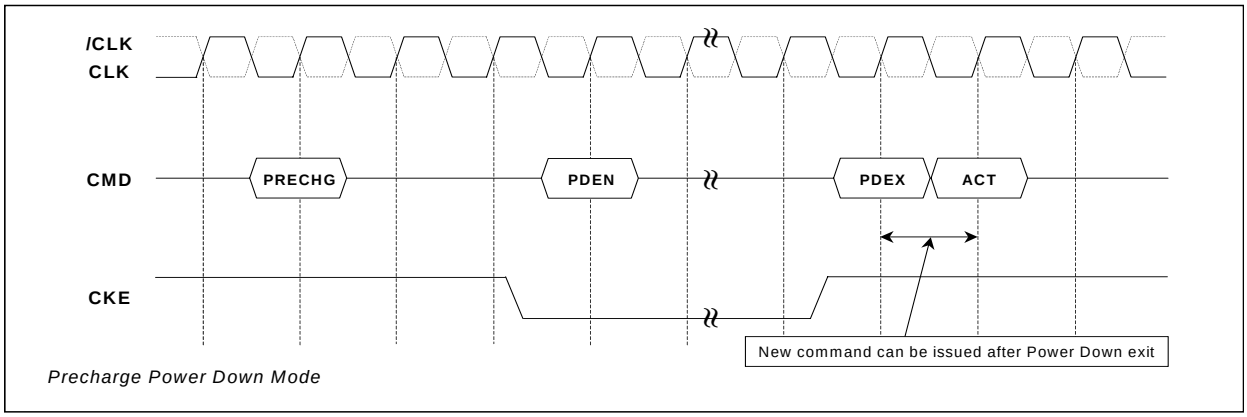
Fig.19. Self Refresh Entry and Exit



Power Down mode

A Power Down mode can be achieved by asserting CKE=L as shown in Fig.20. There are two kinds of Power Down mode: 1. Active and 2. Precharge Power Down mode. The device must be in idle state and all banks must be closed before CKE assertion in Precharge Power Down mode. Active Power Down mode can be initiated in row active state. The device will exit Power Down mode when CKE is sampled high at the rising edge of the clock.

Fig.20. Power Down mode

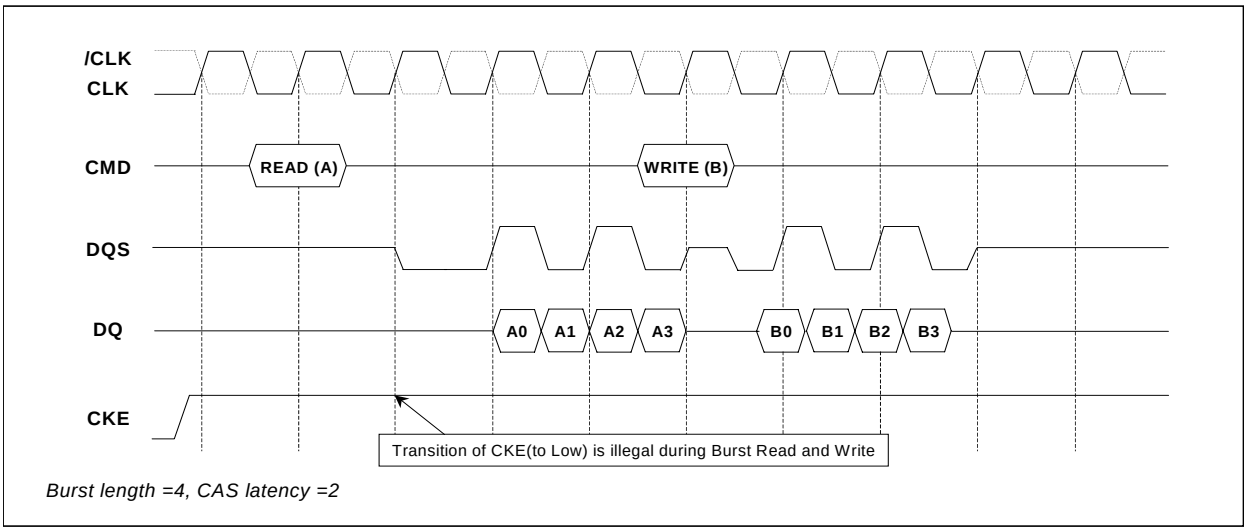


Precharge Power Down Mode

CKE function

Since clock suspend mode in SDR SDRAM cannot be used in DDR SDRAM, it is illegal to issue CKE=L during read or write burst.

Fig.21. CKE function



Burst length =4, CAS latency =2

IDD TEST CONDITIONS (TA=0 to 70 °C, Voltage referenced to VSS = 0V)

Test Condition	Symbol
Operating Current: One bank; Active - Precharge; tRC=tRC(min); tCK=tCK(min); DQ,DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	IDD0
Operating Current: One bank; Active - Read - Precharge; Burst Length=2; tRC=tRC(min); tCK=tCK(min); address and control inputs changing once per clock cycle	IDD1
Precharge Power Down Standby Current: All banks idle; Power down mode; CKE=Low, tCK=tCK(min)	IDD2P
Idle Standby Current: Vin>=Vih(min) or Vin=<Vil(max) for DQ, DQS and DM	IDD2N
Idle Standby Current: /CS=High, All banks idle; tCK=tCK(min); CKE=High; address and control inputs changing once per clock cycle. VIN=VREF for DQ, DQS and DM	IDD2F
Idle Quiet Standby Current: /CS>=Vih(min); All banks idle; CKE>=Vih(min); Addresses and other control inputs stable, Vin=Vref for DQ, DQS and DM	IDD2Q
Active Power Down Standby Current: One bank active; Power down mode; CKE=Low, tCK=tCK(min)	IDD3P
Active Standby Current: /CS=HIGH; CKE=HIGH; One bank; Active-Precharge; tRC=tRAS(max); tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	IDD3N
Operating Current: Burst=2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); IOUT=0mA	IDD4R
Operating Current: Burst=2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle	IDD4W
Auto Refresh Current: tRC=tRFC(min) - 8*tCK for DDR200 at 100Mhz, 10*tCK for DDR266A & DDR266B at 133Mhz; distributed refresh tRC=tRFC(min) - 14*tCK for DDR400 at 200Mhz	IDD5
Self Refresh Current: CKE =< 0.2V; External clock on; tCK=tCK(min)	IDD6
Operating Current - Four Bank Operation: Four bank interleaving with BL=4, Refer to the following page for detailed test condition	IDD7
Random Read Current: 4banks active read with activate every 20ns, AP(Auto Precharge) read every 20ns, BL=4, tRCD=3, IOUT=0 mA, 100% DQ, DM and DQS inputs changing twice per clock cycle; 100% addresses changing once per clock cycle	IDD7A

DETAILED TEST CONDITIONS FOR DDR SDRAM IDD1 & IDD7

IDD1: Operating current: One bank operation

1. Typical Case: VDD = 2.5V, T=25 °C for DDR200, 266, 333; VDD = 2.6V, T=25 °C for DDR400
2. Worst Case: VDD = 2.7V, T= 0 °C
3. Only one bank is accessed with tRC(min), Burst Mode, Address and Control inputs on NOP edge are changing once per clock cycle. Iout = 0mA
4. Timing patterns
   - DDR200(100Mhz, CL=2): tCK = 10ns, CL2, BL=2, tRCD = 2*tCK, tRC = 10*tCK, tRAS = 5*tCK
     Read: A0 N R0 N N P0 N A0 N - repeat the same timing with random address changing
     50% of data changing at every burst
   - DDR266B(133Mhz, CL=2.5): tCK = 7.5ns, CL=2.5, BL=4, tRCD = 3*tCK, tRC = 9*tCK, tRAS = 5*tCK
     Read: A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing
     50% of data changing at every burst
   - DDR266A (133Mhz, CL=2): tCK = 7.5ns, CL=2, BL=4, tRCD = 3*tCK, tRC = 9*tCK, tRAS = 5*tCK
     Read: A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing
     50% of data changing at every burst
   - DDR333(166Mhz, CL=2.5): tCK = 6ns, CL=2, BL=4, tRCD = 3*tCK, tRC = 10*tCK, tRAS = 7*tCK
     Read: A0 N N R0 N N N P0 N N A0 N - repeat the same timing with random address changing
     50% of data changing at every burst
   - DDR400(200Mhz, CL=3): tCK = 5ns, CL=3, BL=4, tRCD = 3*tCK, tRC = 11*tCK, tRAS = 8*tCK
     Read: A0 N N R0 N N N N P0 N N - repeat the same timing with random address changing
     50% of data changing at every burst

     Legend: A=Activate, R=Read, W=Write, P=Precharge, N=NOP

IDD7: Operating current: Four bank operation

1. Typical Case: VDD = 2.5V, T=25 °C for DDR200, 266, 333; VDD = 2.6V, T=25 °C for DDR400
2. Worst Case: VDD = 2.7V, T= 0 °C
3. Four banks are being interleaved with tRC(min), Burst Mode, Address and Control inputs on NOP edge are not changing. Iout = 0mA
4. Timing patterns
   - DDR200(100Mhz, CL=2): tCK = 10ns, CL2, BL=4, tRRD = 2*tCK, tRCD= 3*tCK, Read with Autoprecharge
     Read: A0 N A1 R0 A2 R1 A3 R2 A0 R3 A1 R0 - repeat the same timing with random address changing
     50% of data changing at every burst
   - DDR266B(133Mhz, CL=2.5): tCK = 7.5ns, CL=2.5, BL=4, tRRD = 2*tCK, tRCD = 3*tCK Read with autoprecharge
     Read: A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing
     50% of data changing at every burst
   - DDR266A (133Mhz, CL=2): tCK = 7.5ns, CL2=2, BL=4, tRRD = 2*tCK, tRCD = 3*tCK
     Read: A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing
     50% of data changing at every burst
   - DDR333(166Mhz, CL=2.5): tCK = 6ns, CL=2.5, BL=4, tRRD = 2*tCK, tRCD = 3*tCK, Read with autoprecharge
     Read: A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing
     50% of data changing at every burst
   - DDR400(200Mhz, CL=3): tCK = 5ns, CL = 2, BL = 4, tRRD = 2*tCK, tRCD = 3*tCK, Read with autoprecharge
     Read: A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing
     50% of data changing at every burst

     Legend: A=Activate, R=Read, W=Write, P=Precharge, N=NOP

AC Overshoot/Undershoot Specification for Address and Control Pins

This specification is intended for devices with no clamp protection and is guaranteed by design

Parameter	Specification
	DDR200/266/333/400
Maximum peak amplitude allowed for overshoot (See Figure 1):	1.5 V
Maximum peak amplitude allowed for undershoot (See Figure 1):	1.5 V
The area between the overshoot signal and VDD must be less than or equal to (See Figure 1):	4.5 V-ns
The area between the undershoot signal and GND must be less than or equal to (See Figure 1):	4.5 V-ns

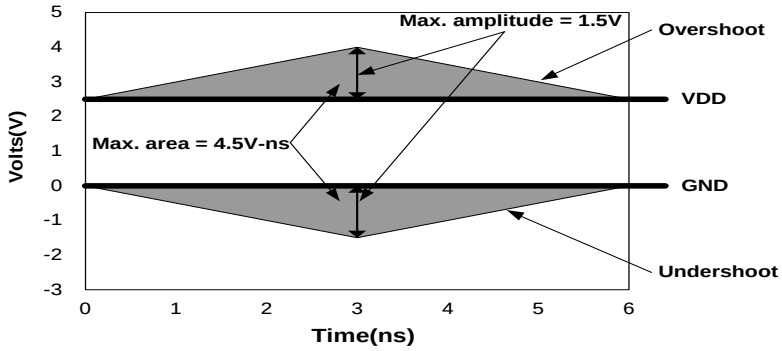


Figure 1: Address and Control AC Overshoot and Undershoot Definition

Overshoot/Undershoot Specification for Data, Strobe, and Mask Pins

Parameter	Specification
	DDR200/266/333/400
Maximum peak amplitude allowed for overshoot (See Figure 2):	1.2 V
Maximum peak amplitude allowed for undershoot (See Figure 2):	1.2 V
The area between the overshoot signal and VDD must be less than or equal to (See Figure 2):	2.4 V-ns
The area between the undershoot signal and GND must be less than or equal to (See Figure 2):	2.4 V-ns

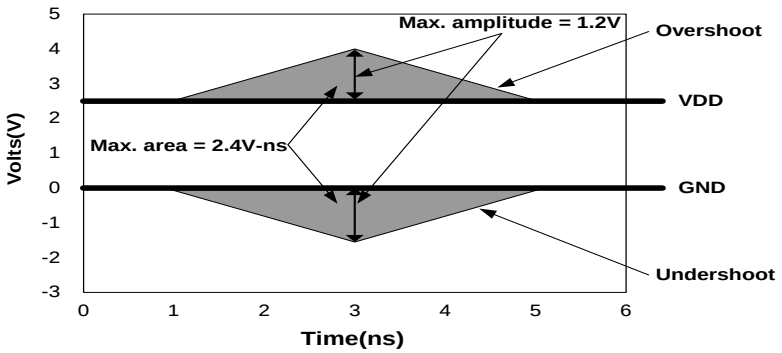
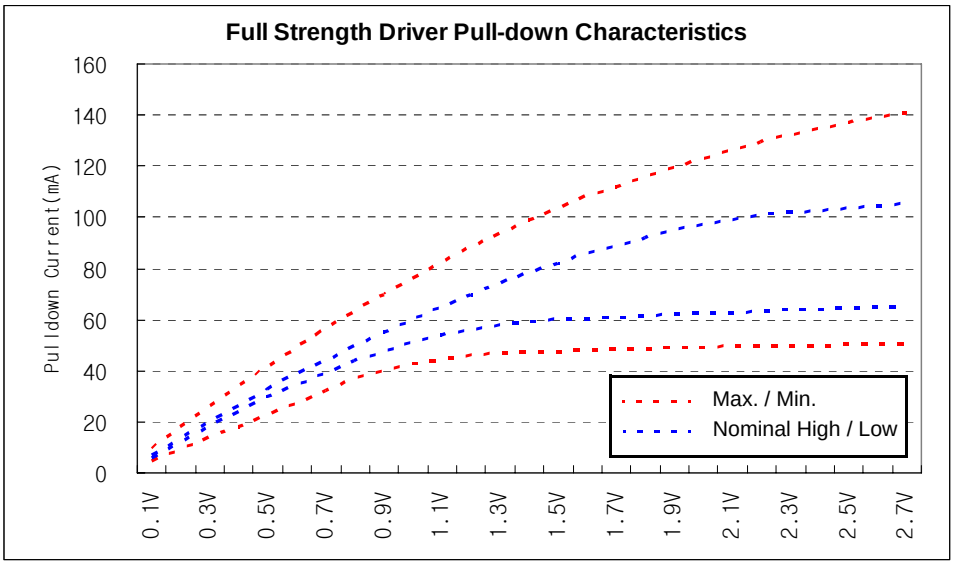


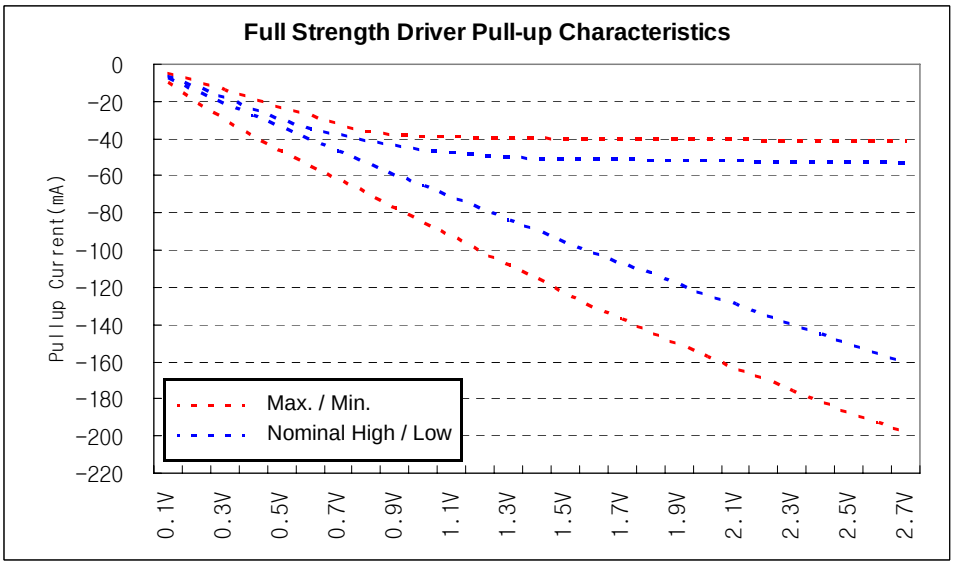
Figure 2: DQ/DM/DQS AC Overshoot and Undershoot Definition

OUTPUT DRIVER CHARACTERISTIC CURVES

Full Strength Output Driver Curves

1. The nominal pulldown V-I curve for DDR SDRAM devices will lie within the inner bounding lines of the V-I curve of below figure. (not guaranteed)
2. The full variation in driver pulldown current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of below figure.
3. The nominal pullup V-I curve for DDR SDRAM devices will lie within the inner bounding lines of the V-I curve of below figure. (not guaranteed)
4. The full variation in driver pullup current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of below figure.



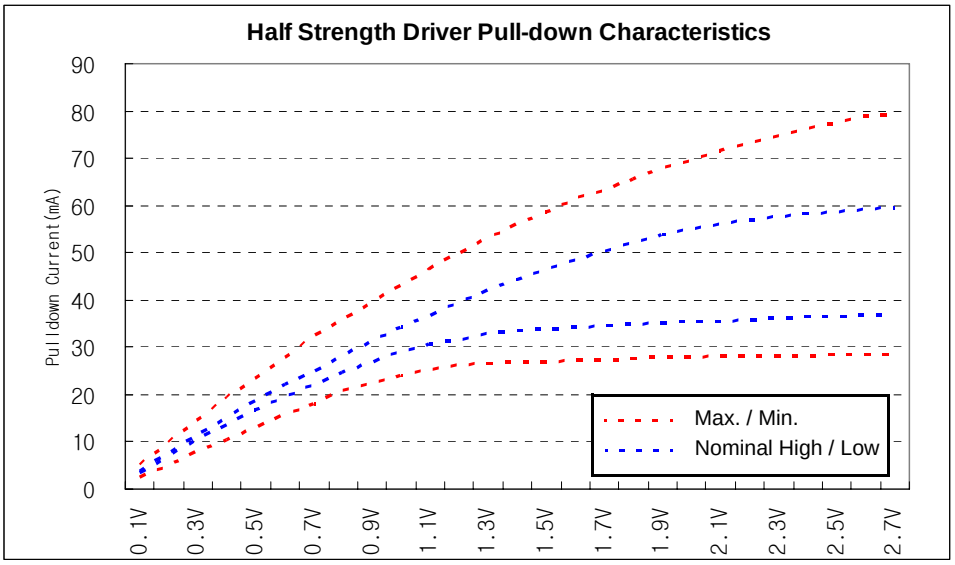


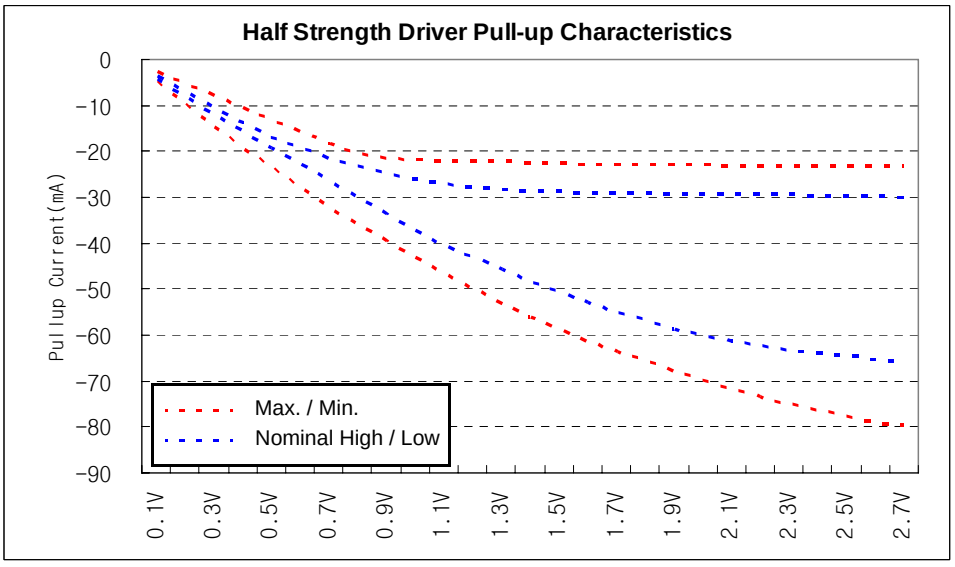
Full Strength Output Driver Characteristics Table

Voltage (V)	Pull-Down Current (mA)				Pull-Up Current (mA)			
	Norm Low	Norm High	Minimum	Maximum	Norm Low	Norm High	Minimum	Maximum
0.1V	6.0	6.8	4.6	9.6	-6.1	-7.6	-4.6	-10.0
0.2V	12.2	13.5	9.2	18.2	-12.2	-14.5	-9.2	-20.0
0.3V	18.1	20.1	13.8	26.0	-18.1	-21.2	-13.8	-29.8
0.4V	24.1	26.6	18.4	33.9	-24.0	-27.7	-18.4	-38.8
0.5V	29.8	33.0	23.0	41.8	-29.8	-34.1	-23.0	-46.8
0.6V	34.6	39.1	27.7	49.4	-34.3	-40.5	-27.7	-54.4
0.7V	39.4	44.2	32.2	56.8	-38.1	-46.9	-32.2	-61.8
0.8V	43.7	49.8	36.8	63.2	-41.1	-53.1	-36.0	-69.5
0.9V	47.5	55.2	39.6	69.9	-43.8	-59.4	-38.2	-77.3
1.0V	51.3	60.3	42.6	76.3	-46.0	-65.5	-38.7	-85.2
1.1V	54.1	65.2	44.8	82.5	-47.8	-71.6	-39.0	-93.0
1.2V	56.2	69.9	46.2	88.3	-49.2	-77.6	-39.2	-100.6
1.3V	57.9	74.2	47.1	93.8	-50.0	-83.6	-39.4	-108.1
1.4V	59.3	78.4	47.4	99.1	-50.5	-89.7	-39.6	-115.5
1.5V	60.1	82.3	47.7	103.8	-50.7	-95.5	-39.9	-123.0
1.6V	60.5	85.9	48.0	108.4	-51.0	-101.3	-40.1	-130.4
1.7V	61.0	89.1	48.4	112.1	-51.1	-107.1	-40.2	-136.7
1.8V	61.5	92.2	48.9	115.9	-51.3	-112.4	-40.3	-144.2
1.9V	62.0	95.3	49.1	119.6	-51.5	-118.7	-40.4	-150.5
2.0V	62.5	97.2	49.4	123.3	-51.6	-124.0	-40.5	-156.9
2.1V	62.9	99.1	49.6	126.5	-51.8	-129.3	-40.6	-163.2
2.2V	63.3	100.9	49.8	129.5	-52.0	-134.6	-40.7	-169.6
2.3V	63.8	101.9	49.9	132.4	-52.2	-139.9	-40.8	-176.0
2.4V	64.1	102.8	50.0	135.0	-52.3	-145.2	-40.9	-181.3

Half Strength Output Driver Curves

1. The nominal pulldown V-I curve for DDR SDRAM devices will lie within the inner bounding lines of the V-I curve of below figure. (not guaranteed)
2. The full variation in driver pulldown current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of below figure.
3. The nominal pullup V-I curve for DDR SDRAM devices will lie within the inner bounding lines of the V-I curve of below figure. (not guaranteed)
4. The full variation in driver pullup current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of below figure.

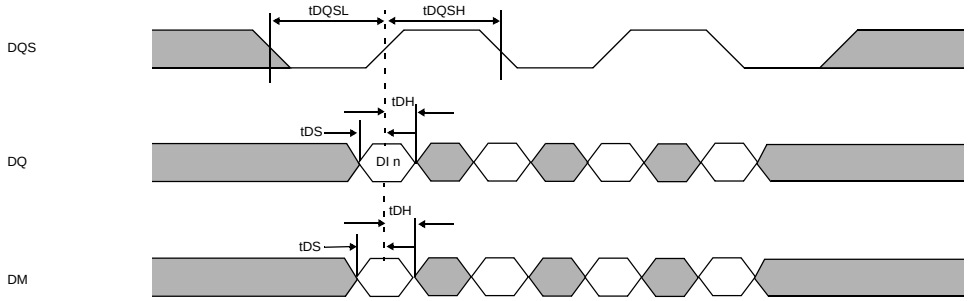




Half Strength Output Driver Characteristics Table

Voltage (V)	Pull-Down Current (mA)				Pull-Up Current (mA)			
	Norm Low	Norm High	Minimum	Maximum	Norm Low	Norm High	Minimum	Maximum
0.1V	3.4	3.8	2.6	5.0	-3.5	-4.3	-2.6	-5.0
0.2V	6.9	7.6	5.2	9.9	-6.9	-8.2	-5.2	-9.9
0.3V	10.3	11.4	7.8	14.6	-10.3	-12.0	-7.8	-14.6
0.4V	13.6	15.1	10.4	19.2	-13.6	-15.7	-10.4	-19.2
0.5V	16.9	18.7	13.0	23.6	-16.9	-19.3	-13.0	-23.6
0.6V	19.6	22.1	15.7	28.0	-19.4	-22.9	-15.7	-28.0
0.7V	22.3	25.0	18.2	32.2	-21.5	-26.5	-18.2	-32.2
0.8V	24.7	28.2	20.8	35.8	-23.3	-30.1	-20.4	-35.8
0.9V	26.9	31.3	22.4	39.5	-24.8	-33.6	-21.6	-39.5
1.0V	29.0	34.1	24.1	43.2	-26.0	-37.1	-21.9	-43.2
1.1V	30.6	36.9	25.4	46.7	-27.1	-40.3	-22.1	-46.7
1.2V	31.8	39.5	26.2	50.0	-27.8	-43.1	-22.2	-50.0
1.3V	32.8	42.0	26.6	53.1	-28.3	-45.8	-22.3	-53.1
1.4V	33.5	44.4	26.8	56.1	-28.6	-48.4	-22.4	-56.1
1.5V	34.0	46.6	27.0	58.7	-28.7	-50.7	-22.6	-58.7
1.6V	34.3	48.6	27.2	61.4	-28.9	-52.9	-22.7	-61.4
1.7V	34.5	50.5	27.4	63.5	-28.9	-55.0	-22.7	-63.5
1.8V	34.8	52.2	27.7	65.6	-29.0	-56.8	-22.8	-65.6
1.9V	35.1	53.9	27.8	67.7	-29.2	-58.7	-22.9	-67.7
2.0V	35.4	55.0	28.0	69.8	-29.2	-60.0	-22.9	-69.8
2.1V	35.6	56.1	28.1	71.6	-29.3	-61.2	-23.0	-71.6
2.2V	35.8	57.1	28.2	73.3	-29.5	-62.4	-23.0	-73.3
2.3V	36.1	57.7	28.3	74.9	-29.5	-63.1	-23.1	-74.9
2.4V	36.3	58.2	28.3	76.4	-29.6	-63.8	-23.2	-76.4
2.5V	36.5	58.7	28.4	77.7	-29.7	-64.4	-23.2	-77.7
2.6V	36.7	59.2	28.5	78.8	-29.8	-65.1	-23.3	-78.8

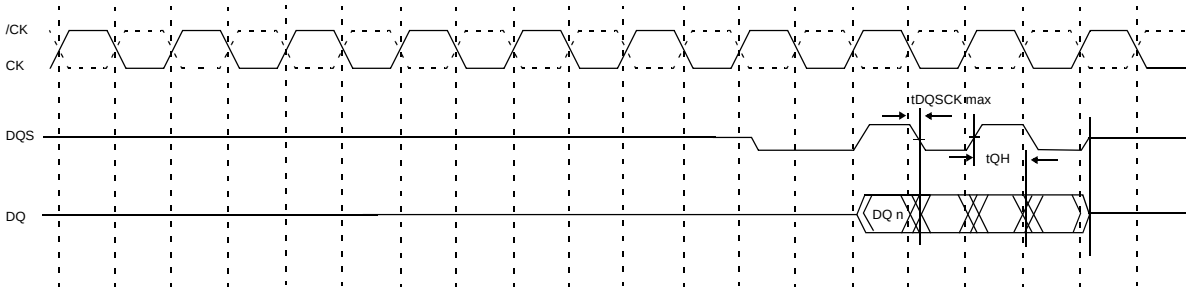
Data Input (Write) Timing (BL=4)



DI n = Data in for column n
3 subsequent elements of data in are applied in the programmed order following DI n

Don't care

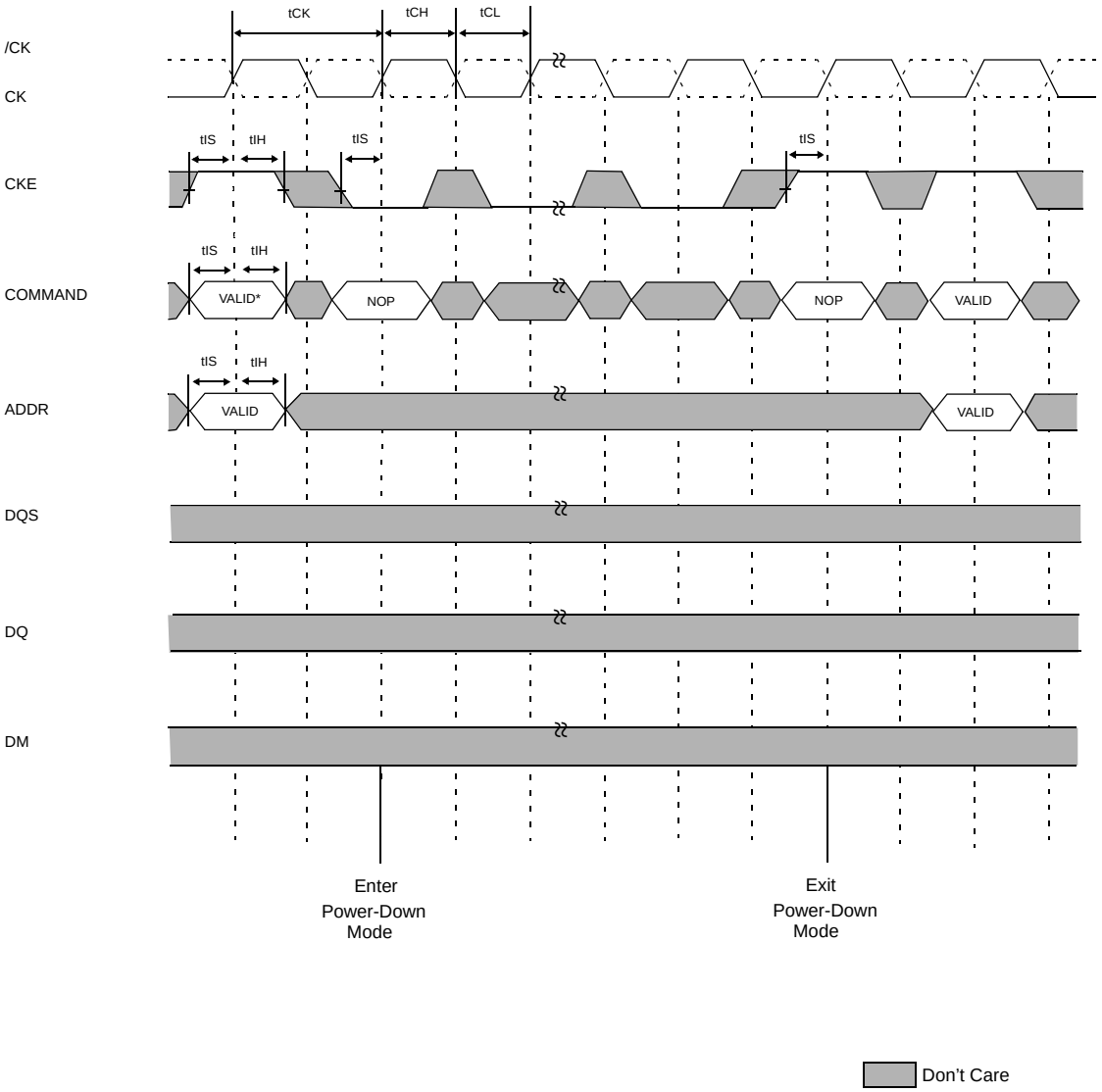
Data Output (Read) Timing (BL=4)



tDQSQ and tQH are only shown once, and are shown referenced to different edges of DQS, only for clarify of illustration.
tDQSQ and tQH both apply to each of the four relevant edges of DQS.

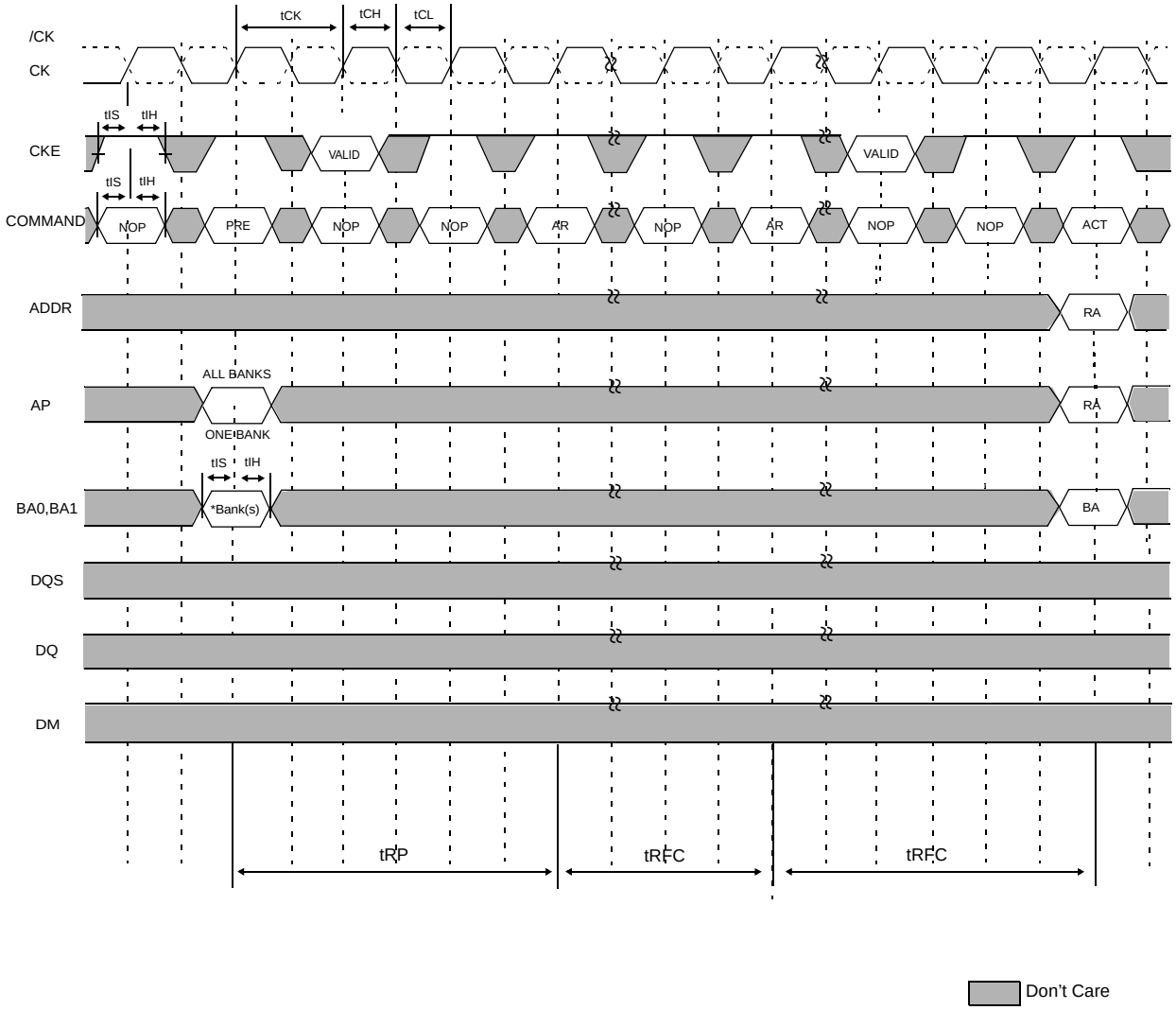
tQHmin = tHPmin - X where;
tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCH, tCL)
X consists of tDQSQmax, the pulse width distortion of on-chip clock circuits, data pin to pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.

Power Down Mode



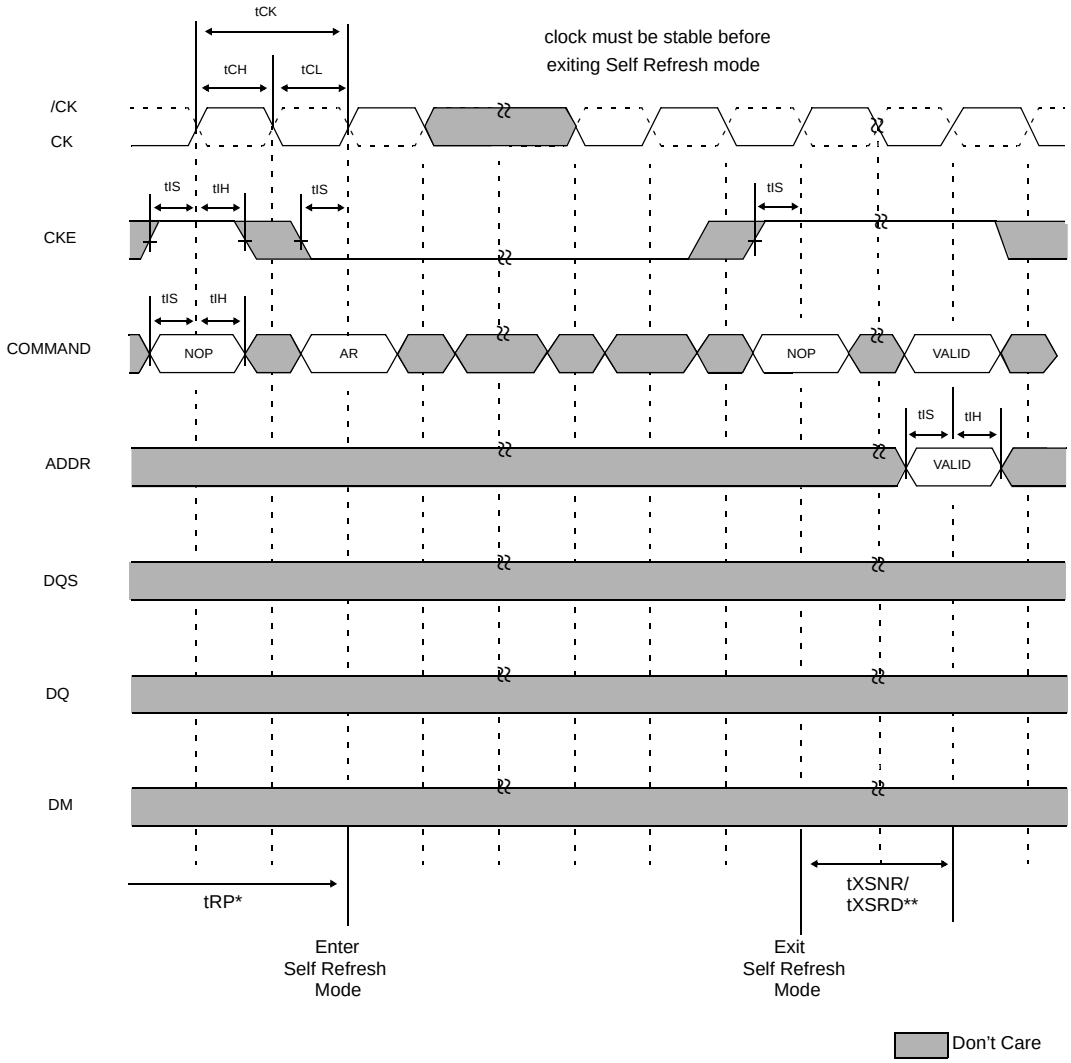
No column accesses are allowed to be in progress at the time Power-Down is entered.
* = If this command is a PRECHARGE (or if the device is already in the idle state) then the Power-Down mode shown is Precharge Power Down. If this command is an ACTIVE (or if at least one row is already active) then the Power-Down mode shown is Active Power Down.

Auto Refresh Mode



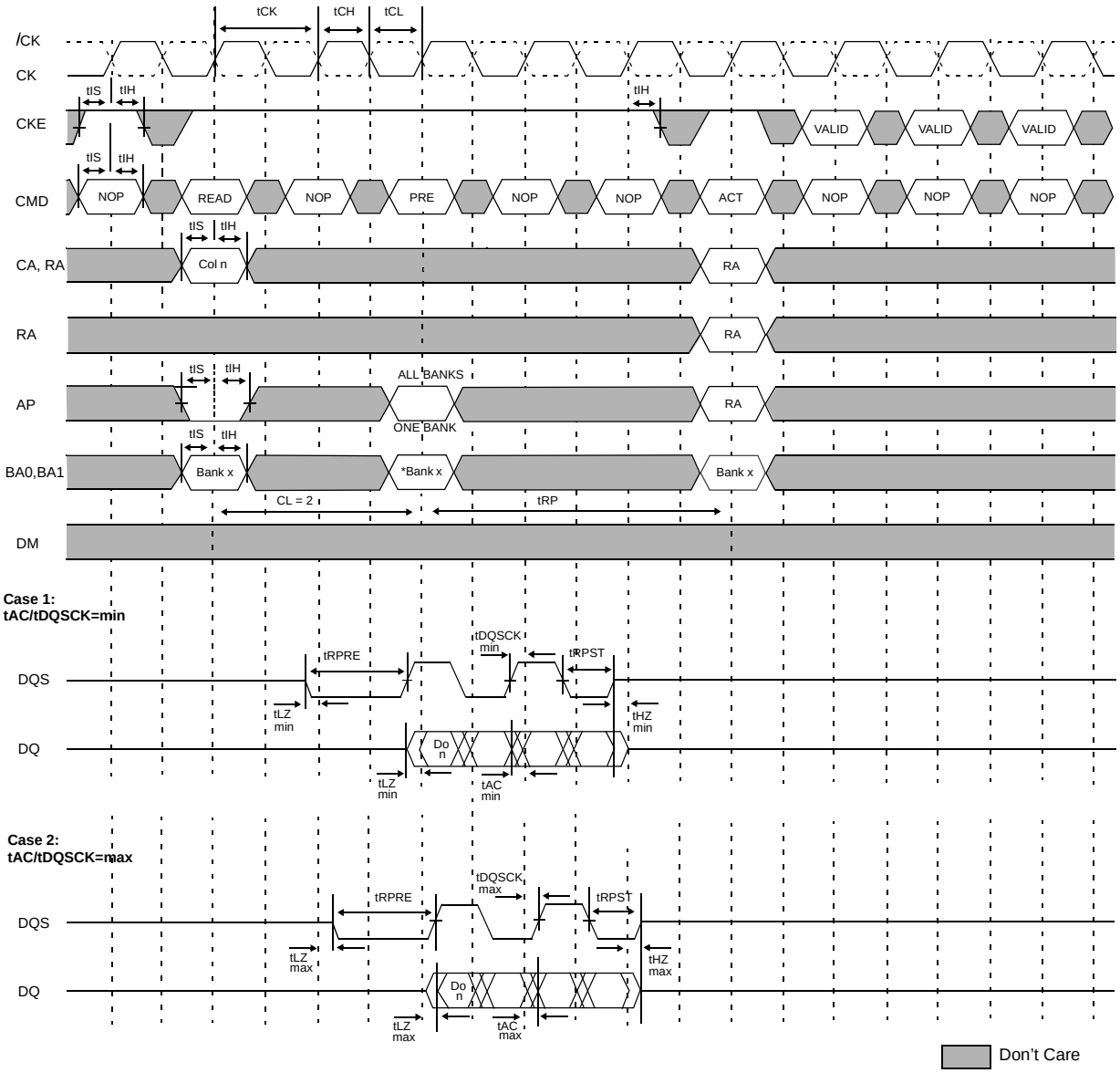
* = " Don't Care ", if AP is High at this point; AP must be High if more than one bank is active (i.e., must precharge all active banks)
PRE = Precharge, ACT = Active, RA = Row Address, BA = Bank Address, AR = Autorefresh.
NOP commands are shown for ease of illustration; other valid commands may be possible at these times.
DM, DQ and DQS signals are all "Don't Care" / High-Z for operation shown.

Self Refresh Mode



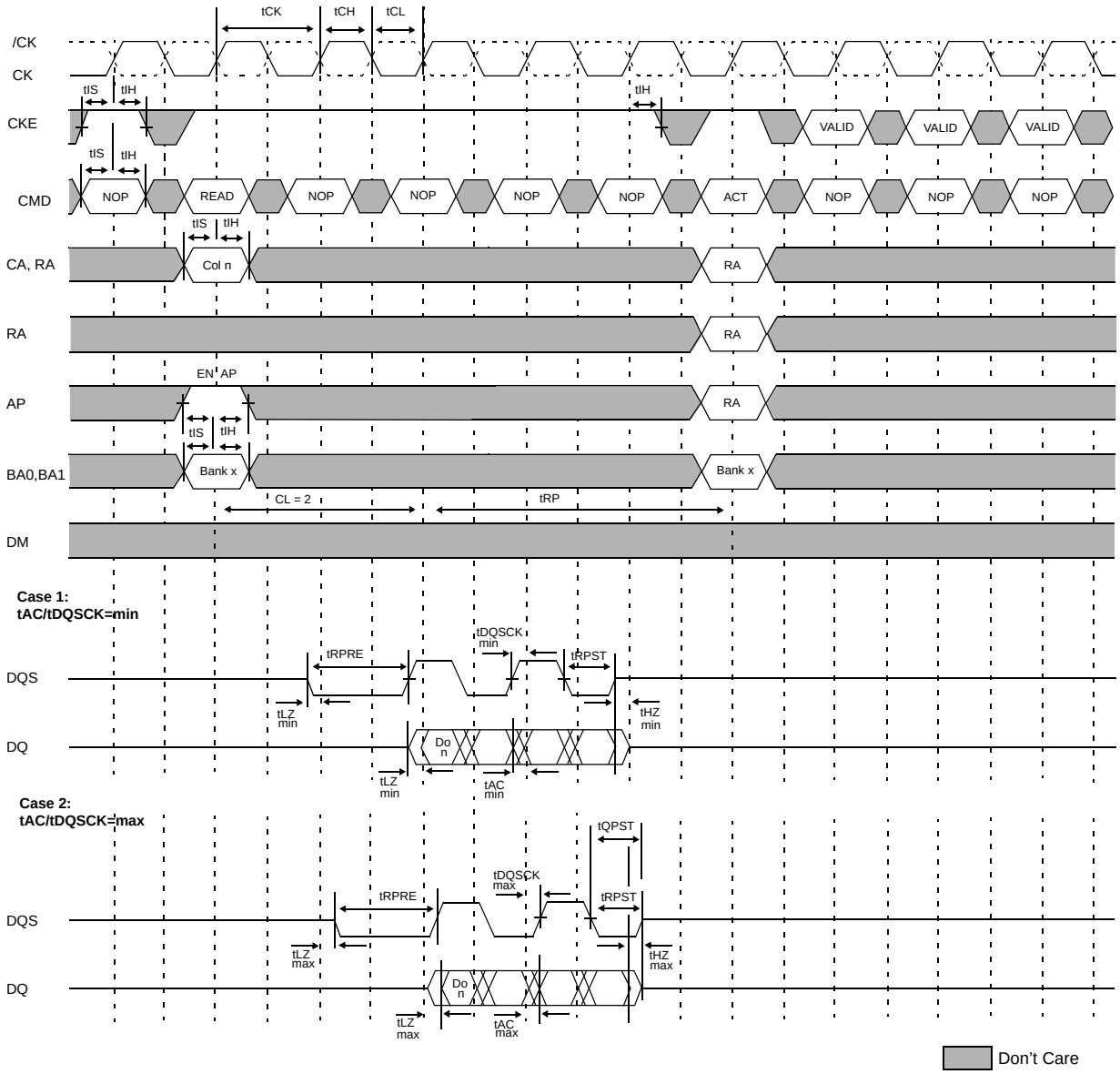
* = Device must be in the "All banks idle" state prior to entering Self Refresh mode
** = tXSNR is required before any non-READ command can be applied, and tXSRD (200 cycles of CK) are required before a READ command can be applied.

Read Without Auto Precharge



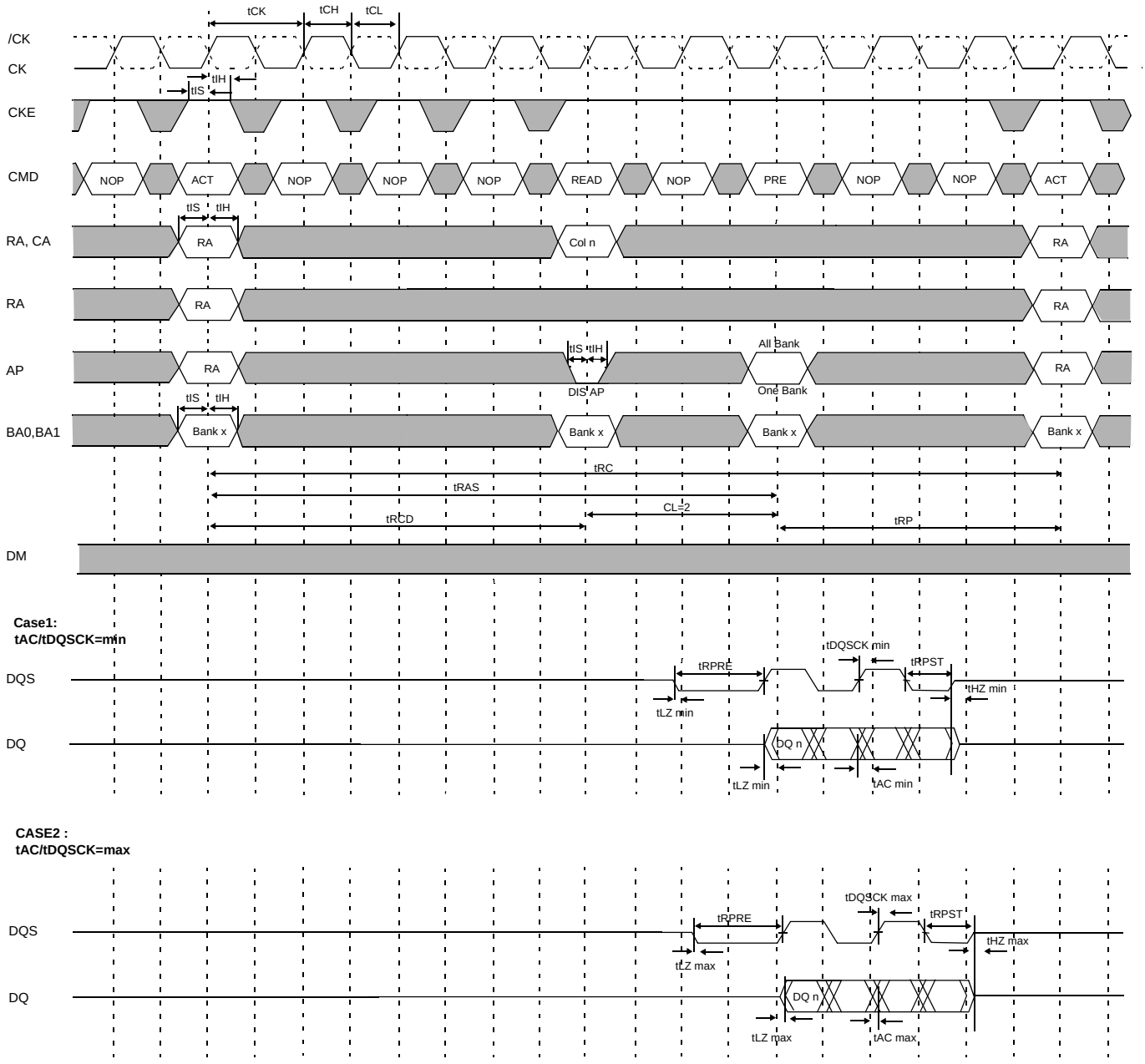
DO n = Data Out from column n
Burst Length = 4 in the case shown
3 subsequent elements of Data Out are provided in the programmed order following DO n
DIS AP = Disable Autoprecharge
* = "Don't Care", if AP is HIGH at this point
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address
NOP commands are shown for ease of illustration; other commands may be valid at these times

Read With Auto Precharge



DO n = Data Out from column n
Burst Length = 4 in the case shown
3 subsequent elements of Data Out are provided in the programmed order following DO n
EN AP = Enable Autoprecharge, ACT = ACTIVE, RA = Row Address
NOP commands are shown for ease of illustration ; other commands may be valid at these times

Bank Read Access



DQ n = Data out from column n
Burst length = 4 in the case shown
3 subsequent elements of Data out are provided in the programmed order following DQ n
DIS AP = Disable Autoprecharge
* = * " Don't Care", if AP is high at this point
PRE = Precharge, ACT=Active, RA=Row Address, BA=Bank Address
NOP commands are shown for ease of illustration; other commands may be valid at these times
Note that tRCD > tRCD min so that the same timing applies if Autoprecharge is enabled (in which case tRAS would be limiting)

Don't care

Revision History

Revision	History	Date
1.0	Initial data sheet released	Oct. 2004
1.1	State Diagram modified	Apr. 2006